AD 298 810

ENGINEERING SERVICES ON
TRANSISTORS

REPORT NO. 10

FIRST QUARTERLY PROGRESS REPORT

PERIOD COVERED: 1 AUGUST TO 31 OCTOBER 1962
DATE OF THIS REPORT: 31 DECEMBER 1962

Contract DA 36-039 sc-90759
(Continuation of Contract DA 36-039 sc-89201)
Order No. 00080-PM-62-91-91 (4939)
DA Project Nos. 3A-99-21-001 and 3A-99-21-002

U. S. Army Electronics Research and Development Laboratory
Fort Monmouth, N. J.

Prepared by Bell Telephone Laboratories, Incorporated
On behalf of Western Electric Company, Incorporated
222 Broadway, New York 38, N. Y.

REPORT NO. 10
ENGINEERING SERVICES ON TRANSISTORS

Report No. 10

ENGINEERING SERVICES ON TRANSISTORS

FIRST QUARTERLY PROGRESS REPORT

Period Covered: 1 August to 31 October 1962
Date of this Report: 31 December 1962

Contract DA 36-039 sc-90759
(Continuation of Contract DA 36-039 sc-89201)
Order No. 00080-PM-62-91-91 (4939)
DA Project Nos. 3A-99-21-001 and 3A-99-21-002
Signal Corps Technical Requirements SCL 7649, Dated 7 November 1961
Signal Corps Technical Requirements SCL 7650, Dated 7 November 1961
Technical Guide Lines PR&C 62-ELP/R-4939, Dated 14 November 1961

U.S. Army Electronics Research and Development Laboratory
Fort Monmouth, N. J.

OBJECT

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, together with their circuit properties and applications, with a view toward demonstrating and increasing the practicability of their use in operating equipment.

This report was prepared by Bell Telephone Laboratories, Incorporated
On behalf of Western Electric Company Incorporated
222 Broadway, New York 38, N. Y.

The following engineers and scientists participated in its preparation:

J. H. Forster
J. Koesis
A. B. Kuper
R. Lindner
K. E. Martersteck
J. T. Nelson
T. B. Ramachandran

SUMMARY OF STATUS

Work on this contract is a continuation of that carried out on Contract DA 36-039 sc-89201, DA 36-039 sc-88931 and earlier contracts of this continuous series.

Status of Tasks 4 and 9 is summarized below. Tasks 1, 2, 3, 5, 6 and 8 have been completed as reported previously under earlier contracts. Task 7 is inactive by mutual agreement. A final report is being prepared on Task 2.

During the period covered by this report, 1 August to 31 October 1962 approximately 1,900 engineering man hours were devoted to work on this contract.

TASK 4 – NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Work on the germanium 1-Gc power transistor and the 3-Gc transistor has continued. Fabrication of 0.25 watt, 1-Gc mesa transistors to supply samples has been started. Several processing problems have been solved so that devices can now be made in a consistent fashion. Power gain at 1 Gc is low and must be improved. Development of the planar interdigitated structure has been reduced because of the increased effort on the mesa structure. Experiments have been carried out on the insulating oxides, indicating pin holes and low breakdown of the oxide after heat treatment. Improved diffusion and evaporation techniques have been initiated in the 3-Gc transistor program. In addition, a study of the use of thermally deposited oxides and photolithographic processes has been started. The use of the new coaxial power header has been delayed because of the difficulty in obtaining properly metalized beryllia insulators. Recently obtained samples have shown improvement and should be adequate for sample headers.

Characterization of the base resistance of the transistors from terminal measurements still remains a problem. To help relate the measurements to the physical structure an analysis has been carried out taking into account the distributed nature of the base resistance and the collector and emitter junction impedance.

Analysis of the general problem of charge distribution in the base and collector barrier regions of microwave transistors has been carried out. Numerical solutions have not yet been obtained.

A direct measurement of avalanche multiplication in transistors has been carried out. Results indicate that multiplication has the same functional form as previously published measurements, but when lightly doped P-type starting material is used (i.e. above 1 ohm-cm) the breakdown voltage may be considerably lower than previously published breakdown data.

TASK 9 – FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Work has been continued on fabrication and evaluation of multiple chip integrated circuits. This has included investigation of exploratory fabrication techniques and design of the chips for use in these circuits.

The evaluation of integrated packages including planar semiconductor and silicon resistor chips is continuing. Measured propagation times for integrated double LLL gates are about six nanoseconds. Work on integration of film resistors with planar semiconductor chips is now being carried out.

A re-evaluation of the multi-junction level shifter operation in the LLL gate has been made. Measurements indicate that use of epitaxial transistors in the LLL gate improves input margins and decreases stored-charge requirements for the level-shifter diode.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION 1 - PURPOSE

The general purpose of this contract is to make studies and investigations related to transistors and transistor-like devices, together with their circuit properties and applications, with a view toward demonstrating and increasing the practicality of their use in operating equipment. This contract is a successor to preceding contracts of a similar nature: Contract W36-039 sc-44497, Contract DA 36-039 sc-5589, Contract DA 36-039 sc-64618, Contract DA 36-039 sc-85352, Contract DA 36-039 sc-88962, Contract DA 36-039 sc-88931, and Contract DA-36-039 sc-89201.

These contracts call for services, facilities, and material to be employed on mutually acceptable tasks. Of the nine tasks assigned, five have been completed with final reports. Work on Task 2, Transistor Reliability was terminated in August 1961. A final report is being prepared. Brief descriptions of other tasks and dates of Final Reports are contained in Section 1 of Report No. 6 dated 31 December 1961, the First Quarterly Report issued under Contract DA 36-039 sc 88931.

Tasks currently active under this contract are outlined below.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

The contractor shall make theoretical and experimental studies leading to exploratory models and, upon mutual agreement, to feasibility designs of:

1. New transistors using new or previously untried principles.
2. New transistors obtained by studied modifications of existing types.

The new transistors shall be primarily intended and suitable for application to voltage, current, and power amplifiers, and to associated electronic transducers.

In general, transistors having ac amplifying properties in the following ranges are of particular interest:

1. Germanium transistors from 1000 mcps to 3000 mcps with as large power ratings as the state of the art permits.
2. Silicon transistors from 100 mcps to 1000 mcps with as large power ratings and as high temperature ratings as the state of the art permits.
3. Devices of other materials with specific attention to obtaining frequency, power, noise, or temperature advantages over germanium and silicon devices.

TASK 4A - MICROWAVE TRANSISTOR

The contractor shall conduct a study and investigation leading to the design and fabrication of a transistor capable of operating with a minimum of 10-db gain at 3000 mc. The transistor structure should be of a diffused-base mesa type with stripe emitter and base electrodes or with dot-emitter and ring-base electrodes. An accurate design theory for such a device shall be established together with an appropriate equivalent circuit including package parameters. It is desired that the transistor be matched into 50-ohm input and output coaxial terminations. From a microwave point of view the structure (package and transistor) shall be basically broadband. Ideally, the transistor should be capable of greater than 10-db power gain from dc to 3000 mc. Appropriate experimental models of such devices including any necessary adapters indicative of the progress made shall be furnished during the course of this program.

TASK 4B - 1000-MC, 1-WATT TRANSISTOR

The contractor shall conduct a study and investigation leading to the design and fabrication of a transistor capable of operating with a minimum of 1 watt of power output at 1000 mc with a minimum gain of 10 db and with a minimum efficiency of 30 per cent, for this power output and gain. An accurate design theory for such a device shall be established together with an appropriate equivalent circuit including package parameters. The structure shall be an hermetically sealed package with provisions for mounting on simple heat sinks. Appropriate experimental models of such devices, including any necessary adapters, indicative of the progress made shall be furnished during the course of this program.

TASK 4C - 2000-MC, 2-WATT TRANSISTOR

The contractor shall conduct a study and investigation leading to the design and development of a transistor capable of operating with a minimum of 2 watts power output at 2000 mcps with a minimum gain of 10 db and with a minimum efficiency of 25 per cent for this power output and gain. An accurate design theory for such a device shall be established together with an appropriate equivalent circuit including package parameters. The structure shall be an hermetically sealed package with provisions for mounting on simple heat sinks. Appropriate experimental models and/or prototype units of such devices, including any necessary adapters, indicative of the progress made shall be furnished during the course of this program.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

The Contractor shall make theoretical and experimental studies leading to exploratory models, and upon mutual agreement, to feasibility designs and finally to development models of semiconductor components able to perform more complex functions than existing components can, thereby reducing the number of components needed in electronic systems with the ultimate objective of improving the reliability and reducing the cost of such systems. The components to be investigated shall include:

1. Functional devices, namely devices designed from physical phenomena to perform as directly as possible desired systems functions.

2. Diodes and transistors in miniature insulated packages to be compatible with thin film resistor-capacitor techniques. These packages may form an integral part of an insulating substrate on which resistive and capacitive films may be evaporated to form complete circuits.

3. Integrated circuits, namely combination of circuit elements including, where appropriate, functional devices designed and fabricated as units to perform desired systems functions.

The work shall include but not be limited to:

1. Evaluation of systems requirements and related components requirements with attention to such figures of merit as speed, gain, power dissipation, impedance, reliability, packing density, interconnection topology, etc. A study shall be undertaken of selected categories of semiconductor components to determine their universality with respect to a variety of systems. For example, integrated diode-transistor logic circuits shall be studied for gating and flip-flop circuits. The gating circuits studied shall be designed for optimum fan-in, fan-out requirements. The fan-in, fan-out requirements should be based upon systems analysis.

2. Study of miniature diodes and transistors in insulated packages shall be undertaken to determine the effects, if any, of the packaging techniques on the performance and reliability of these devices. Wherever possible, comparative conventional devices shall be used to make this analysis most meaningful.

3. Fabrication of these selected exploratory components and circuits to determine their figures of merit. For example, four-layer, three-terminal device structures (PNPN) having turn-off gain properties shall be investigated for application to functional circuits. In addition, the contractor shall endeavor to determine the reliability inter-relationship of several semiconductor devices (i.e. diodes and transistors) contained in a common sealed package or several junctions fabricated in a common semiconductor wafer.

4. The cost factors associated with all of the above shall be investigated, particularly with respect to yield on multiple devices in common package or multiple junctions within one wafer.

SECTION 2 - ABSTRACT

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Chapter 1 reports the status of the microwave germanium transistors. Fabrication of 0.25-watt, 1-Gc mesa transistors has been started to supply samples. The processing problems and the method of attack are reviewed in the chapter. Problems of oxide breakdown in the planar structure, the modifications of evaporation techniques to improve the oxides, and the possible use of photolithographic techniques and thermally deposited oxides are also treated. Reduction of base resistance by two base diffusions, a heavy diffusion under the base stripes and between the stripes, and a normal diffusion under the emitter is suggested.

In Chapter 2 it is shown that the base resistance of the power transistor is substantially influenced by the shunting effect of the forward-biased emitter junction impedance, and the feedback capacitance of the collector junction. The problem is analyzed as distributed resistances and capacitances closely approximating the physical structure of the device. Results indicate a complex base impedance should be used in the equivalent circuit characterizing the device.

The problem of charge distribution in the base and collector barrier regions of microwave transistors is treated in Chapter 3. Existing solutions of transport of carriers in devices and the boundary conditions for the solutions are reviewed. These boundary conditions are no longer valid for the microwave transistor. A solution with less restrictive boundary conditions is proposed. Modification of the Einstein equation relating the diffusion constant and mobility of carriers so that it is applicable in regions of high electric fields has been carried out.

Chapter 4 presents data on avalanche multiplication in diffused-base germanium transistors. Collector and base currents of the transistor are measured as a function of collector voltage with the emitter forward-biased. Surface currents are measured with the emitter reverse-biased and are subtracted from the total currents. Correction is made for modulation of the currents due to base layer narrowing. Results indicate agreement in functional form with published data, but a significantly lower avalanche breakdown voltage must be used for collector with doping 2 ohm-cm.

Alloy transistor multiplication and the breakdown voltage agrees with published data. The lower breakdown found in diffused-base transistors is not the result of microplasmas, but appears to be a true large area effect.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

In Chapter 5 the present status of the integrated circuits and functional devices program is briefly reviewed. The program now includes work on integration of

diffused-silicon resistors or thin-film resistors with planar diffused-silicon devices. Measurements of propagation delay time for integrated LLL gates including silicon resistors are discussed. Delays of about six nanoseconds are indicated. Operation of the multi-junction diode level shifter in LLL gates is reviewed. It is concluded that satisfactory input margins for many applications are afforded with a double junction level shifter used with an epitaxial 2N914 transistor. Use of the 2N914 also reduces the charge storage requirement on the level shifter.

SECTION 3 - PUBLICATIONS AND REPORTS

No publications or other reports were issued during this contract period.

SECTION 4 - FACTUAL DATA

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Chapter 1

STATUS OF THE MICROWAVE TRANSISTORS

By J. T. Nelson

1.1 INTRODUCTION

During this quarter, technical effort has continued on the development of the 1-watt, 1000-mc transistor and the low-power 3-kmc transistor. Fabrication of an intermediate-power mesa transistor, similar to the one described in a previous report, has again been picked up in order to supply samples.

The work during this quarter has largely been concerned with processing problems. The problems and the method of attack are covered in this chapter.

1.2 FABRICATION OF INTERMEDIATE POWER TRANSISTORS

A mesa transistor capable of delivering 225 mw at 1 Gc was reported previously (Ref. 1). Fabrication of additional units of this type which could be nominally rated as 0.25 watt at 1 Gc has again been started. Up to this time the results have been unsatisfactory. The mesa structure used is similar to that previously reported with 1 x 10-mil electrodes with 0.2-mil spacing between electrodes and a base-layer thickness between 0.25 and 0.5 microns.

During this quarter, 12 evaporation runs have been initiated. From these starts approximately 20 units have been encapsulated. All of the units have unsatisfactorily low gain at 1 Gc. The base resistance of these transistors appears to be substantially higher than predicted from the structure of the device, with resulting lower power gain than anticipated. Further analysis of the base-resistance problem has been carried out in order to further understand the problem (Chapter 3 of this report).

During the early part of the quarter, when fabrication procedures were being established in the model laboratory, the loss of devices during processing was very

high. Results were unpredictable so that it was difficult to carry a systematic program to improve the device performance at high frequencies. Techniques for rejection of devices with potentially unsatisfactory dc characteristics at an early stage of fabrication have been improved and processing has been substantially improved. Losses have been substantially reduced so that it should now be possible to concentrate effort on the improvement of the high-frequency performance of the transistor.

It is now known that the principal problem in the fabrication was the result of dicing the slabs into individual wafers. The collector reverse current and collector breakdown voltage of all transistors were found to be substantially degraded between an initial test on the slab after evaporation and alloying of the electrodes and final test on a finished transistor. Damage to the collector junction has been isolated to the dicing of the slab. Both scribing and breaking, and sawing were used to separate the wafers. Although the same care was used to dice these transistors that has previously produced good transistors of other types, damage to the collector junction resulted without fail. This problem has arisen on the power transistor because the combined requirements of large stripe dimensions to handle the operating current and small wafer size to minimize the inductance of connections to the header results in a nominal distance of 0.004 inches between the collector junction and the edge of the wafer. Separation of the wafers by etching has not been instituted and the damage to the collector junction is no longer a problem.

Low collector breakdown and devices whose collector junctions collapse under applied bias as a result of defective epitaxial material still present a problem. More careful selection of epitaxial material has improved this situation although further improvement in the quality of the epitaxial material is necessary.

Loss during lead bonding is decreasing as operators gain experience.

Electrical characterization of the devices has indicated that the gain at 1 Gc is too low to be used as a practical amplifier. The gain also falls off rapidly as the signal level is increased so that the power output is limited. Further investigation is underway to determine why the transistors produced recently have not been satisfactory.

1.3 PLANAR INTERDIGITATED STRUCTURE

Development effort on the planar interdigitated structure has been reduced because of the increased effort on the mesa structure. A limited investigation of the breakdown in evaporated oxides has been carried out. A sandwich of base electrode material (Ag-Au-Sb) silicon monoxide, and the aluminum electrode material (Al) was evaporated to simulate the electrode structure. Breakdown of the oxide was approximately 10 volts per 1000 Å. After the structure was heated to the emitter alloying temperature, approximately 450° C, and cooled, the breakdown dropped to 1 volt per 1000 Å.

An experiment consisting of etching of silver through an evaporated silicon monoxide film has indicated a high density of pin holes in the evaporated oxide films.

A study of the use of cerium oxide as an evaporated insulating layer was also started. The choice of this material is based on the fact that evaporated layers are almost completely CeO_2 which is a stable form of the oxide at room temperature, in contrast to silicon monoxide which is composed of a mixture of SiO_2, unstable

SiO, and silicon. A sandwich similar to that used to test the silicon monoxide has yielded a breakdown of 25 volts per 1000 Å after the alloying heat cycle. However, if a positive potential was applied to the aluminum electrode the rupture could be healed so that the breakdown was in excess of 100 volts per 1000 Å. This effect is not understood, but it is indicative of electrolysis or migration of metal through the oxide. Further study of oxides is obviously necessary.

Additional work in both evaporation techniques and the use of thermally deposited oxides has been carried out in conjunction with the low-power 3-kmc transistor. This work will be applicable to the power structure.

1.4 THE 3-GC TRANSISTOR

The proposed structure requires a 0.25-mil dot emitter and concentric base ring with a spacing from the emitter of less than 0.2 mil.

Development of this transistor has been limited to further process improvement. Work is continuing on refinement of evaporation techniques. A scheme of reducing base resistance by the use of two base-diffusion steps is being investigated, and the use of photolithographic techniques for controlling surface geometry is being studied.

A Vac-Ion evaporation station is being set up for use in processing this transistor. This is being done for two reasons. The general cleanliness and higher vacuum obtainable with this type evaporator should result in more controllable processing. In the evaporation of oxides it is necessary to keep the substrate at a low temperature to prevent scattering of the oxide into the region where the emitter electrodes will be evaporated. In an oil-pumped station oil condenses on the low temperature substrates.

A new set of evaporation jigs for holding the germanium slab and evaporation mask are being designed. They will be made from germanium to eliminate shifts of the germanium wafer with respect to the mask due to differences in thermal expansion during the bakeout cycle. It is desirable to give the germanium a thorough bakeout to clean the surface before evaporation. This causes electrode registry problems with the presently used molybdenum jig and nickel mask.

The use of a wick-type source has been developed to evaporate the metal electrodes. Used with silver and gold, an effective evaporation source diameter of 0.050" has been obtained which results in more clearly defined electrode geometry.

The narrow separation between the emitter and base ring is required to keep that part of the base resistance resulting from the resistance of the diffused-base layer between the electrodes to an acceptable level. A technique for reducing this portion of the base resistance is being investigated. It is hoped that this technique will both reduce the total base resistance of the device and make necessary less restrictive mechanical tolerances.

An alternate scheme, using photolithographic techniques, is being studied for use in making the 3-Gc structure. The work done until this quarter has been principally limited to the use of evaporated oxides through stencil-type masks. There is some evidence that thermally deposited oxides may suffer less from pin holes and leakage problems than the evaporated oxides. Photolithographic techniques now appear capable of producing the closely controlled geometries necessary for this

structure. For these reasons, a study of the feasibility of the use of photo techniques and thermally deposited oxides has been started. In addition to the advantages that have been stated there would be a decided advantage in manufacturing with this technique since processing would then be more closely allied to silicon-transistor production.

1.5 NEW POWER COAXIAL HEADER

Plans called for the use of the new coaxial header, described in the previous quarterly report, during this quarter. Fabrication of these headers has been delayed by poor adherence of the molybdenum-manganese metalized layer to the beryllium oxide insulator. Metalized insulators have been supplied by an outside supplier. The first samples obtained yielded bond strengths of between 500 and 1000 pounds per square inch, with the break between the metalized layer and the ceramic. Additional effort by the supplier has not produced insulators with bond strengths of 2500 pounds per square inch with partial fracture of the metal ceramic bond and partial fracture of the ceramic. Although this bond strength is well below that of a good ceramic metal seal the parts are adequate for initial models of the header.

This difficulty has been attributed to difficulty in metalizing high-purity beryllia (99+% BeO). The high-purity beryllia was chosen for this encapsulation because of its high thermal conductance. At the time of the choice of this material, metalizing problems were not anticipated. Additional insulators of a lower-purity beryllia, containing a glass phase to ease the metalizing problem, have been ordered and should be obtained during the next interval. A penalty of poorer heat transfer must be paid if it is necessary to use the lower-purity insulator. At this time it is not known what the thermal conductivity of these insulators will be.

An active metal solder (Titanium-BT) has also been used for making the bonds. The result has been severe weakening of the ceramic in the vicinity of the bond and rupture strengths of less than 250 pounds per square inch have resulted. In all cases the ceramic has yielded in the vicinity of the bond.

REFERENCE

1. Engineering Services on Transistors, Report No. 5, Contract DA 36-039 sc-88962, 3 August, 1962.

Chapter 2

HIGH FREQUENCY BASE IMPEDANCE ANALYSES OF MICROWAVE TRANSISTORS

By J. Kocsis

2.1 INTRODUCTION

For most practical applications a one-dimensional theory is adequate for characterizing transistors, and equivalent circuits based on the one-dimensional theory are in common use today. As the frequency limit of junction transistors has been extended to higher and higher frequencies, the distributed nature of certain transistor structures had to be taken into account and the one-dimensional theory was no longer adequate. One of the early transistors for which this was true was the grown-junction transistor. The grown-junction transistor has been analyzed by means of a simplified two-dimensional theory by R. L. Pritchard (Ref. 1) with the conclusion that it can be represented for small-signal ac application by an ideal transistor (transistor without extrinsic elements) and a complex, frequency-dependent, base impedance Z_b. Evaluations of microwave mesa transistors give similar results; i.e. the distributed nature of transistor parameters must be taken into account even in a first order approximation and its effect can be represented by an impedance Z_b.

The purpose of this chapter is to extend Pritchard's two-dimensional theory to diffused-base mesa or planar transistors with stripe emitter and base contacts and to determine the base impedance of these transistors.

2.2 DISCUSSION

2.2.1 Analysis

The over-all performance of a device is determined by the combined effects of the minority and majority current flow upon applied voltages on the input and output terminals. In this chapter the effect of majority current flow through the base region, emitter depletion layer and collector depletion layer will be analyzed. Elements added to the equivalent circuit due to the effect of majority current flow will be called extrinsic elements, because their effects are essentially added to the transistor action of the internal or ideal transistor.

The structure to be considered is a three-stripe mesa structure, but the conclusions are equally valid for any multiple-stripe structures. In the analyses to be carried out the following assumptions are made:

1. Small-signal ac conditions are assumed.
2. The conductivities of the base and emitter stripes are much larger than the average base conductivity.
3. The effect of the collector series resistance is neglected.
4. Negligible surface and volume recombination in the base; therefore, the base current is due to the high frequency (1 - α) current and to the feedback current.
5. A p-n-p transistor is considered. The results are equally valid for n-p-n devices with the appropriate change in signs.

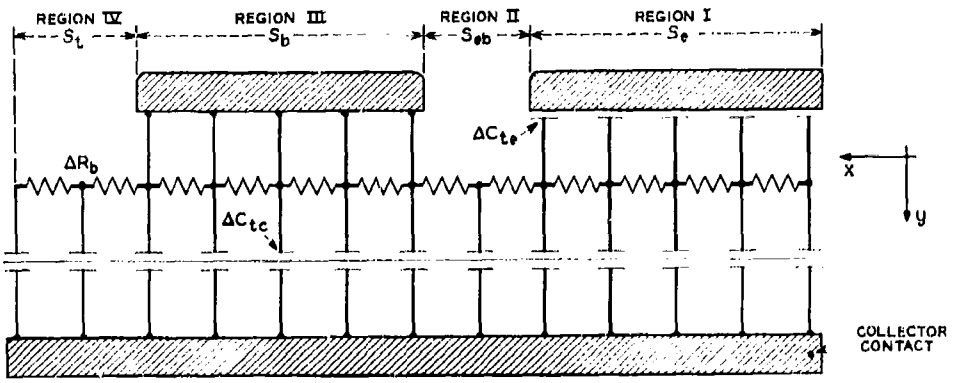

Fig. 1 - Distributed elements in the mesa structure

Fig. 1 shows the half cross section of the structure with the distributed extrinsic elements. In obtaining the distributed equivalent circuit for the extrinsic elements, it was assumed that the base stripe, emitter stripe, and collector contacts are equipotential parts of the structure and the collector series resistance is zero. For the purpose of the analysis the structure is divided into different regions as shown in Fig. 1, each of which is considered separately.

Region I

The problem in this case is similar to that of the grown-junction transistor, where the effective base lies between the emitter and collector junctions of equal size. In analyzing this region, a simplified two-dimensional analysis will be carried out, i.e. in the longitudinal direction (y axis in Fig. 1) only minority carrier flow is considered, neglecting the effect of the emitter depletion layer capacitance C_{te} and collector depletion layer capacitance C_{tc}. In the transverse direction (x axis) only majority carrier flow is considered. Thus, the two-dimensional pattern is separated into two one-dimensional problems. Then, finally, the effect of C_{te} and C_{tc} is considered.

In the following analysis the common-emitter configuration will be used because it considerably simplifies the analysis.

Assume that the ideal common-emitter transistor (emitter and collector depletion layer capacitances and the transverse base resistance are zero) is represented by the following h parameters.

$$[h_e] = \begin{bmatrix} h_{ie} & h_{re} \\ h_{fe} & h_{oe} \end{bmatrix}$$

Assume now that the transverse base resistance is not zero, i.e. $R_b \neq 0$ and the transistor is represented by h'_e

$$[h'_e] = \begin{bmatrix} h'_{ie} & h'_{re} \\ h'_{fe} & h'_{oe} \end{bmatrix} \tag{1}$$

It can be easily shown that (Ref. 1)

$$h_{re} = h'_{re} \tag{2}$$

$$h_{oe} = h'_{oe} \tag{3}$$

$$h_{re} = h'_{fe} \tag{4}$$

In the measurement of h'_{ie} a base-emitter voltage is applied and thus the phase and amplitude of the base current are effected by the transverse base resistance.

Hence, in the common-emitter configuration only h'_{ie} must be determined with the inclusion of a distributed transverse base resistance into the transistor structure. The other three h parameters obtained on the basis of a one-dimensional theory correctly represent the transistor, including the effects of the distributed base resistance between the emitter and collector junctions.

For h'_{ie} the following expression has been obtained by R. L. Pritchard on the basis of the two-dimensional theory

$$h'_{ie} = \frac{R_b}{\Gamma \cdot s_e} \coth \Gamma \cdot s_e \tag{5}$$

where R_b is the transverse base resistance

$$\Gamma^2 = \frac{R_b \cdot y_c}{s_e^2} \tag{6}$$

y_c is the sum of the common-base short-circuit admittance parameters for the ideal transistor, i.e.

$y_e = y_{ib} + y_{rb} + y_{fb} + y_{ob}$

s_e is the emitter stripe width.

The input parameter h'_{ie} arbitrarily can be separated into two parts, one of which is the short-circuit input impedance h_{ie} and the remainder will be called base impedance denoted by Z_b, therefore

$$Z_b = h'_{ie} - h_{ie} \quad . \tag{7}$$

Substituting Equation (5) into Equation (7) and taking $y_e = y_{ie} = \frac{1}{h_{ie}}$, Equation (8) is obtained.

$$Z_b = \frac{R_b}{\Gamma \cdot s_e} \coth \Gamma \cdot s_e - h_{ie} \tag{8}$$

where

$$\Gamma \cdot s_e = (R_b \cdot y_{ie})^{1/2} \quad . \tag{9}$$

After the above separation, h'_e can be written in the following form

$$[\, h'_e \,] = \begin{bmatrix} Z_b + h_{ie} & h_{re} \\ h_{fe} & h_{oe} \end{bmatrix} \tag{10}$$

Equation (10) implies that the transistor can be represented by an ideal model and a Z_b admittance in series with the base.

The effect of depletion layer capacitances has been neglected up to now. The emitter depletion layer capacitance ΔC_{te} is part of the distributed structure in the same way as the corresponding admittance (Δy_{te}) of the forward-biased emitter-base junction. A part of the majority current in the base which is due to the $(1-\alpha)$ current can bypass the base resistance through Δy_{te} and as a consequence of this a complex base impedance arises as given in Equation (8). In the same way ΔC_{te} which is parallel with Δy_{te} in the infinitesimally small part of the structure can contribute to a bypassing path, or in the microwave range its effect can be more significant than y_{te}. Since ΔC_{te} is parallel in the distributed structure with Δy_{te}, the admittance due to ΔC_{te} can be added to $\Sigma \Delta y_{te} = y_{te}$ and the input admittance thus becomes

$$y'_{te} = y_{te} + j\omega C_{te} \quad . \tag{11}$$

It is significant to note that the bypassing effect of C_{te} in the forward direction contributes to a linearly increasing current in the transverse direction.

Similarly, a linear current distribution is obtained due to $(1-\alpha)$ current and therefore the inclusion of ωC_{te} parallel with y_{ie} satisfies the bypassing effect of C_{te} in series with Z_b equally as well in the forward direction as in the reverse direction. Therefore, if C_{te} is taken into account, Equation (8) becomes

$$Z_b = \frac{R_b}{\Gamma' \cdot s_e} \coth \Gamma' \cdot s_e - \frac{1}{y_{ie} + j\omega C_{te}} \tag{12}$$

where

$$\Gamma' \cdot s_e = [R_b (y_{ie} + j\omega C_{te})]^{1/2} \tag{13}$$

The bypassing effect of the reverse-biased collector depletion layer has been neglected which corresponds to the assumption that

$$\Delta R_b \ll \frac{1}{\omega \cdot \Delta C_{tc}} . \tag{14}$$

The feedback current which is present in the base due to C_{tc} can be assumed to have the same effect as the $1-\alpha$ current, i.e. every infinitesimally small transistor in the transverse direction contributes the same amount of feedback current which can flow through the bypassing effect of y'_{te} and R_b to the base terminal in much the same way as the $1-\alpha$ current. For the above reason the base impedance Z_b can be considered to be the same for the feedback current arising through C_{tc}, and C_{tc} can be connected from collector to base of the ideal transistor.

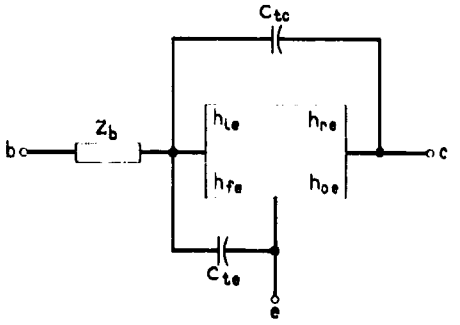

Fig. 2 - Equivalent circuit for Region I

In Fig. 2 the final equivalent circuit is shown for Region I, including the effect of majority current flow in the base region, the bypassing effect of the forward-biased emitter-base junction, and the feedback effect of C_{tc}. In the further analysis of this region consideration will be given to the evaluation of Z_b.

Let us now consider Z_b given by Equation (12). Equation (13) can be written as follows:

$$| \Gamma' \cdot S_e | = K^{1/2} \tag{15}$$

where

$$K \equiv \left| \frac{R_b}{\frac{1}{y_{ie} + j\omega C_{te}}} \right| . \tag{16}$$

Equation (12) can be easily simplified under two conditions: if $K \ll 1$ and if $K \gg 1$. From Equation (16) it is apparent that $K \ll 1$ corresponds where the transverse base resistance is much smaller than the admittance represented by the forward-biased emitter-base junction. This condition can be satisfied at low frequencies where the bypassing effect of the capacitances can be neglected and/or at low current level when the real part of the common-emitter input admittance $Re\ y_{ie}$ is too small to contribute to a bypassing route for the base current. If $K \ll 1$, then Equation (12) simplifies to the well known form

$$Z_b = \frac{R_b}{3} . \tag{17}$$

The other limiting case is when $K \gg 1$. This condition can be due to two reasons, either the frequency is very high and therefore $\omega(C_{te} + C_b)$ is large compared to $1/R_b$ and/or the emitter current is high so that

$$\frac{R_b}{Re\left(\frac{1}{y_{ie}}\right)} \gg 1 .$$

At low frequencies Equation (12) can be simplified to

$$Z_b = R_b \left(\frac{\coth K^{1/2}}{K^{1/2}} - \frac{1}{K} \right) = \frac{R_b}{B} \tag{18}$$

where

$$B \equiv \left(\frac{\coth K^{1/2}}{K^{1/2}} - \frac{1}{K} \right)^{-1}$$

$$K = \frac{R_b}{Re\ (y_{ie})} . \tag{19}$$

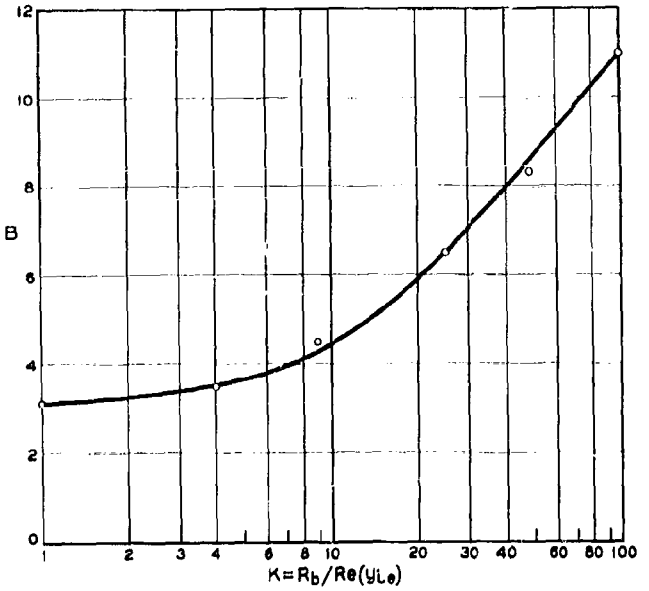

Fig. 3 - Effective base resistance when $Re(y_{ie}) \ll \omega(C_{te} + C_b)$, $Z_b = R_b/B$

In Fig. 3, B vs. $K = \dfrac{R_b}{Re\ (y_{ie})}$ is plotted. This graph shows that for $K \leq 2$, the approximation that the base resistance is $\dfrac{R_b}{3}$ holds. For higher values of K, however, the base resistance is reduced considerably due to the bypassing effect of $Re\ (y_{ie})$. Fig. 3 also shows that the base resistance will be current dependent for power transistors if K is large compared to unity because the value of $Re\ (y_{ie})$ is current dependent. This effect can result in a serious matching problem because of the dependence of R_b on ac current level.

A simplified high frequency approximation for Z_b can be obtained when $Re\ (y_{ie}) \gg j\omega(C_{te} + C_b)$ and $K \gg 1$. Under this condition

$$Re\ (Z_b) = \frac{R_b}{3} \tag{21}$$

$$Im(Z_b) = \frac{1}{j\omega \frac{1}{5}\ (C_{te} + C_b)} \tag{22}$$

where C_b is the base-charging capacitance.

At frequencies much lower than the cutoff frequency obtained by the base transit time

$$Re\ (y_{ie}) = \frac{1}{r_e\ \beta_o} \tag{23}$$

where β_o is the low-frequency common-emitter current gain and

$$r_e = \frac{kT}{q} \cdot \frac{1}{I_e} \tag{24}$$

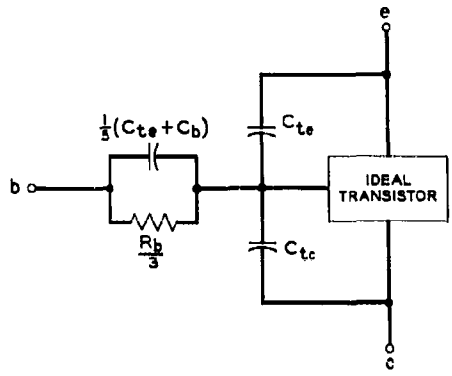

Fig. 4 - Lumped circuit representation for Region I assuming that $K \gg 1$ and $\mathrm{Re}(y_{ie}) \gg \omega (C_{te} + C_b)$

The equivalent circuit of Fig. 2 can be simplified to Fig. 4 with the substitution of Equations (21) and (22), if $h_e (y_{ie}) \gg j\omega(C_{te} + C_b)$ and $K \gg 1$. Unfortunately, the microwave power transistors do not always satisfy the above assumption and then the lumped circuit representation shown in Fig. 4 is not valid. A single frequency or a narrow band simplified R-C representation for Equation (12) must then be used.

Region II

This bulk is outside the emitter junction and therefore the total majority current from Region I will flow across it. There is an additional feedback current from the collector contact which flows through the distributed R_b-C_{tc} network. This region can be incorporated in the equivalent circuit of Region I, therefore, by connecting the distributed $R_b C_{tc}$ network in series with the base as shown in Fig. 5.

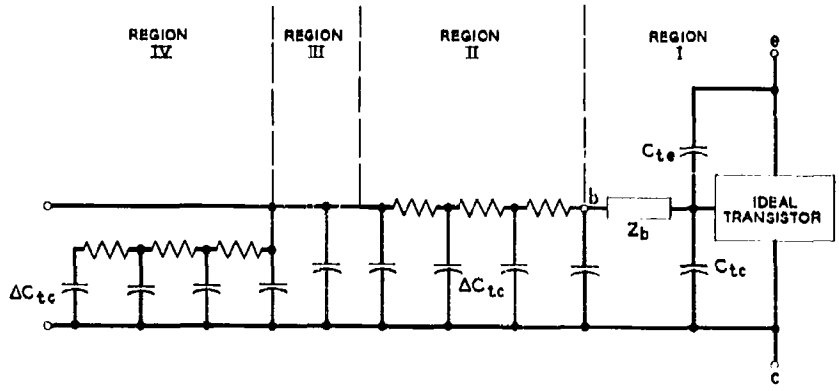

Fig. 5 - Distributed equivalent circuit of Fig. 1

Region III

Since the base stripe has a conductivity much larger than that of the base underneath and $S_b \gg W$, the bulk of the base current from Regions I and II will flow into the edge of the base stripe adjacent to the emitter. It follows that the part of the transverse base current under the base stripe can be omitted. There remains the collector-base capacitance representing the feedback current to the base stripe which can be incorporated into the equivalent circuit as a parallel capacitance to the collector and base terminals.

Region IV

This region is defined by the remaining area of the collector junction and base. It is similar to Region III. The transverse base resistance has to be taken into account, however, because feedback current flows in the transverse direction. This region therefore can be incorporated into Fig. 5 parallel with the collector and base terminals.

Fig. 5 shows the equivalent circuit of the mesa structure with distributed R-C elements. Further simplification of this equivalent circuit is necessary for practical use. The R-C distributed transmission line shown in Fig. 6 can be represented by a symmetrical π equivalent as shown in Fig. 7 (Ref. 2) where

R is the transverse series resistance per unit length,

C is the shunt capacitance per unit length, and

d is the length of the transmission line.

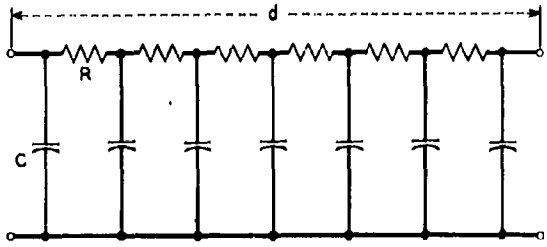

Fig. 6 - Distributed R-C transmission line

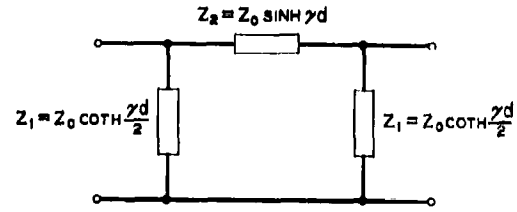

Fig. 7 - π circuit representation of Fig. 6

If $\sqrt{R \cdot j\omega c} \ll 1$, the series expansion of the hyperbolic functions can be used. Neglecting the higher power terms yields the lumped circuit representation shown in Fig. 8. By substituting the lumped π network into Fig. 5, assuming that Region IV is represented by a lossless capacitance and that in the feedback time constant the capacitive effect of Region II is negligible, Fig. 9 is obtained. The limited space here does not allow detailed analysis but it can be shown that for practical devices the assumption used does not represent significant error in the equivalent circuit presentation.

In the analysis only half of the structure has been considered. The other half of the structure can be considered as an identical parallel transistor, therefore, for the three-stripe structure Fig. 10 can be simply obtained.

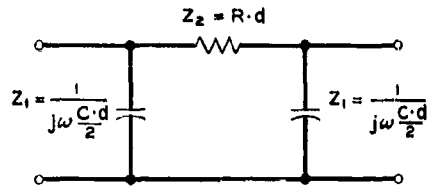

Fig. 8 - Lumped circuit representation of Fig. 7

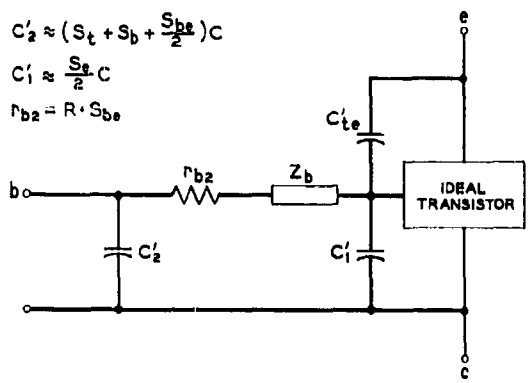

Fig. 9 - Equivalent circuit for half of the three-stripe structure

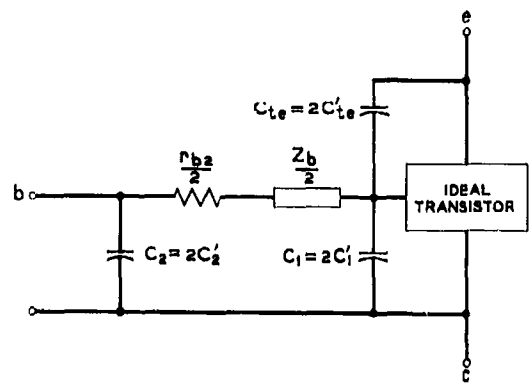

Fig. 10 - Equivalent circuit for the three-stripe structure

2.2.2 Measurements on M2260 High Frequency Power Transistors

Detailed evaluation of the analyses presented have not been completed. Some measurements have been made, however, which indicate the importance of some of the points raised in the analyses.

The following measurement results are given for only one M2260 transistor. Improved parameters have been obtained with some modification; the results, however, give an insight into the problems involved.

DC measurements have been made between the two base stripes (emitter open circuited) and between the emitter and the parallel base stripes resulting (see Fig. 11)

$$2R_{b1} + 2R_{b2} = 110\Omega$$

$$\frac{R_{b2}}{2} = 4\,\Omega\,.$$

From the two measurements $R_{b2} = 8\Omega$ and $R_{b1} = 47\Omega$, the dc or low-frequency base resistance, assuming there is no bypassing effect due to $Re\,(y_{ie})$,

$$r_b = \frac{R_{b1} + \frac{R_{b2}}{3}}{2} = 11.8\Omega\,.$$

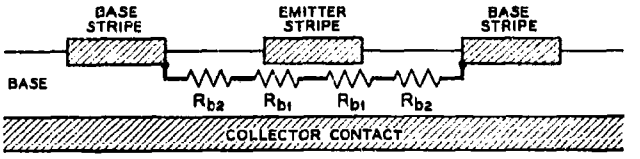

Fig. 11 - DC base resistance of the three-stripe mesa structure

For the same transistor $\beta_o = 18$. Assume $I_e = -100$ ma, then for half the structure

$$\frac{1}{Re\,(y_{ie})} = \beta_o \cdot r_e = 180.52 = 9.4\,\Omega$$

$$K = \frac{R_{b1}}{\beta_o r_e} = \frac{47}{9.4} = 5.$$

From Fig. 3 it can be seen that the bypassing effect of $Re\,(y_{ie})$ is not very important at $I_e = -100$ ma, but it becomes very significant if I_e is further increased.

The C_{ie} is approximately 50 pf ($C_b \ll C_{ie}$), which at $f = 1$ Gc/s, represents $-j3.2\,\Omega$. Its value is thus close to that of $\frac{1}{Re\,(y_{ie})}$ at I_e of -100 ma. As a consequence of the above, the simple frequency independent approximation is not valid at large currents.

In order to determine the high-frequency base impedance, h'_{rb} has been measured as a function of frequency at $I_e = -50$ ma. The results of the measurements are given in Fig. 12.

From Fig. 13

$$h'_{rb} = j\omega C_1 \cdot Z_b \tag{25}$$

assuming that the effect of the internal parameters on h'_{rb} is negligible and

$$|Z_b| \ll \frac{1}{\omega C_1} \cdot \tag{26}$$

Assume that Z_b is represented by a parallel r_b and C_B network then

$$Im(h'_{rb}) = j\omega C_1 \cdot r_b \frac{1}{1 + \omega^2 C_B^2 r_b^2} \tag{27}$$

$$Re(h'_{rb}) = \frac{\omega^2 C_B \cdot C_1 \cdot r_b^2}{1 + \omega^2 C_B^2 r_b^2} \tag{28}$$

$$\text{If } \omega^2 C_B^2 r_b^2 \gg 1 \tag{29}$$

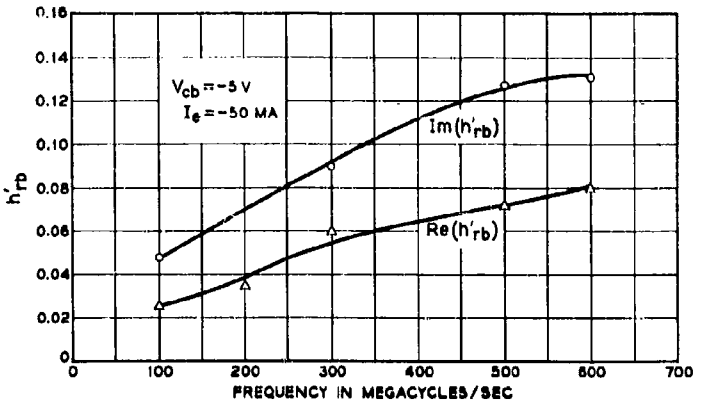

Fig. 12 - h'_{rb} versus frequency for the M2260 transistor

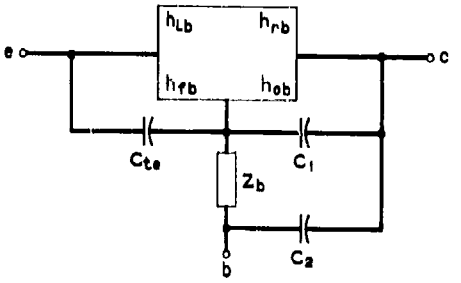

Fig. 13 - Equivalent circuit for the mesa structure

then

$$Im\,(h'_{rb}) \quad \frac{C_1}{\omega C_B^2 r_b} \tag{30}$$

$$Re\,(h'_{rb}) \quad \frac{C_1}{C_B} \tag{31}$$

Fig. 12 shows that $Re\,(h'_{rb})$ approaches a value of approximately 0.1 as the frequency increases. Therefore

$$\frac{C_1}{C_B} \approx 0.1$$

$$C_1 = 1.2 \text{ pf at } V_{cb} = -5 \text{ v}$$

and therefore

$$C_B \approx 12 \text{ pf.}$$

Assuming the approximation given in Equation (22)

$$C_B \approx \frac{1}{5} (C_{te} + C_b)$$

$$C_{te} + C_b \approx 60 \text{ pf.}$$

C_{te} has been measured directly giving 50 pf, which is in good agreement with the 60 pf obtained for C_{te} and C_b. In the calculation, lead inductance effect has been neglected; therefore, measurements have not been made over 600 mc/sec where lead inductance effects are significant.

It is useful to note that if only $Re(Z_b)$ were significant, i. e. just base resistance present, then $Re(h'_{rb}) \approx 0$ and $Im(h'_{rb}) = j\omega C_1 \cdot r_b$. The large, real part of h'_{rb} indicates that a significant phase change occurs probably due to Z_b.

2.3 CONCLUSIONS

The bypassing of the transverse base resistance by $C_{te} + C_b$ at high frequencies and by $Re(y_{ie})$ at high current levels has been evaluated. It is shown that due to the bypassing effect of $Re(y_{te})$ significant change can result in the base resistance, therefore the base resistance can vary as the function of ac current level causing current dependent nonlinearity. At very high frequencies the bypassing effect of $C_{te} + C_b$ gives rise to a capacitive phase and amplitude change in the base resistance which under special cases can be represented by a parallel RC network.

A lumped equivalent circuit representation has been presented for the three-stripe base structure on the basis of Pritchard's two-dimensional analysis. The calculations show that for the microwave power transistor significant amplitude and phase change can occur in the base impedance which have to be taken into account in the power gain calculation. Measurement results are presented for the M2260 power transistor which show that significant change can result in Z_b at high current levels and/or high frequencies.

REFERENCES

1. R. L. Pritchard, "Two-Dimensional Current Flow in Junction Transistors at High Frequencies," Proc. IRE, June 1958.

2. F. E. Terman, "Radio Engineers' Handbook".

Chapter 3

STORED CHARGE IN THE BASE LAYER OF TRANSISTORS

By T. B. Ramachandran

3.1 INTRODUCTION

One of the fundamental quantities associated with a device like a transistor is the control charge stored in the base (including the transition region). Knowledge of the variation of this control charge with current and voltage is necessary to predict the detailed properties of the device. The equations governing the minority (or majority) carrier distribution in low electric field regions are well known. These have been solved by various authors (Refs. 1, 2, 3) under some restrictive conditions.

A review of various assumptions and validity of the resulting solutions is given in this chapter. Some of the problems encountered in removing the restrictive conditions are enumerated.

As an initial step, the condition of approximate space charge neutrality has been relaxed and a program for numerical solution for the carrier density distribution is in preparation. This chapter describes, qualitatively, the nature of the expected solutions.

In the appendix, the validity of the low field equations for current and Einstein's relationship is examined.

Considerations are restricted to a one-dimensional p-n-p transistor.

3.2 CRITIQUE OF THE PRESENT TRANSISTOR THEORY

The equations that determine the current flow and the carrier densities in low electric field regions are

$$J_p = q\mu_p p E - q D_p \nabla p \tag{1}$$

$$J_n = q\mu_n n E - q D_n \nabla n \tag{2}$$

$$\nabla \cdot J_p + \frac{p - p_n}{\tau_p} q = q \frac{\partial p}{\partial t} \tag{3}$$

$$E = \frac{q}{\epsilon} (p + N - n) \tag{4}$$

where the symbols have the usual meaning and $N = N(x)$ is the impurity density.

A general analytical solution to these equations is impossible because of the nonlinearity of the resulting differential equations. An analytical solution may be obtained under some simplifying approximations.

The simplest approximation, valid at very-low current densities, is that the electric field due to injected carrier densities may be neglected. Thus for $N = N_d$, a constant, Shockley obtained the solution

$$p = Ae^{x/L_p} + Be^{-x/L_p}$$

where A and B are arbitrary constants and $L_p = \sqrt{D_p \tau_p}$ is the diffusion length. For an exponential impurity distribution, the solution has been given by Kromer (Ref. 4).

Webster (Ref. 2) and Rittner (Ref. 3) extended the low-level theory by neglecting recombination in the base and assuming the electron current in the base to be zero.

The electric field in the base due to the carrier densities follows from the latter assumption and is

$$\frac{qE}{kT} = -\frac{1}{n}\frac{dn}{dx}$$

Assuming, further, quasi space charge neutrality, the solution for $N = N_d$, a constant, is

$$2\frac{p}{N_d} - \log\left(1 + \frac{p}{N_d}\right) = C - \frac{J_p x}{q D_p N_d}$$

where C is an arbitrary constant.

For any other impurity distribution, numerical solutions only are possible.

To obtain a particular solution, we require

(1) the width of the base for which the solution is valid and

(2) the boundary values for the carriers.

For the normal operation of the transistor, the width of the base-emitter space charge region may be neglected. Thus, the effective quasi-neutral base width W is $W = W_B - X_{mb}$ as illustrated in Fig. 14. The boundary values at the edges of the quasi-neutral region are obtained by assuming that the injected carrier density at the edges is proportional to $e^{qV/kT}$, where V is the forward bias across the junction. For a reverse-biased junction, V is negative and with $|V| \gg kT/q$, the carrier density is nearly zero.

In a simple way, we may show that a zero carrier density requires an infinite carrier velocity for a finite current. For, if V is the carrier velocity, the current density may be written

$$J_p = qpV$$

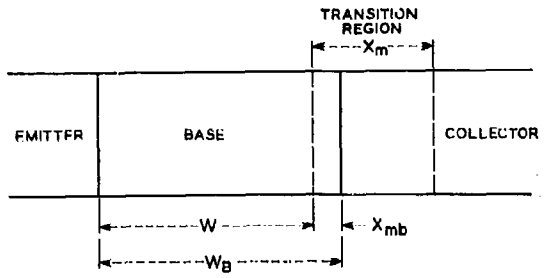

Fig. 14 - Simplified one-dimensional transistor

Thus, for $p = 0$, $V \rightarrow \infty$ for a finite J_p. This reasoning applies equally to dc and ac solutions.

The theory outlined above worked well for large base width transistors since the carrier transit time across the transition region was negligible in comparison with the neutral base transit time. These two transit times are comparable for small base width transistors.

As a first approximation, we may assume with Early (Ref. 5) that the carrier density p_o is constant throughout the transition region and given by

$$p_o = J_p/q\,V_{max}$$

where V_{max} is the scatter limited velocity. The carrier transit time τ_t in a region of width X_m, then, is

$$\tau_t = \frac{X_m}{2V_{max}}$$

X_m in the first approximation is considered to be voltage dependent only. The dependence of X_m on current has been considered by Kirk to explain the fall-off of common-emitter unity gain frequency f_T at high currents.

It is shown in the appendix that in high electric field regions such as the collector barrier region, the carrier distribution function deviates substantially from its thermal equilibrium value. In such a case, we have to consider the diffusion component of the total current also. Thus, while Early's approximation may be valid at low currents, it appears that extension to high currents is not justified.

3.3 EXTENSION OF THE PRESENT THEORY

The preceding modification of the present theory by Early has been used to predict f_T of high frequency mesa transistors. A considerable discrepancy exists between the measured and the predicted values. Also, influence of the collector impurity density on the parameters of the transistor (except insofar as the width of the transition region is concerned) is not known. Thus, a numerical solution to the Equations (1) through (4) without the approximation of a quasi-neutral base region is desirable.

Since our attention is to be focussed mainly on high frequency transistors, we may, without serious error, neglect recombination in the base layer and assume $\tau_p \rightarrow \infty$. Also, the assumption of zero electron current in the base is a satisfactory one.

For a straight-forward numerical solution of the problem, we would have as boundary conditions known value of carrier densities at the emitter and collector ohmic contacts. Such an attack is precluded by the fact that an infinite time would be required, in the absence of any criterion for the choice of first and second derivatives of carrier densities at the ohmic contact, to obtain the proper solution.

The assumption of zero electron current in the base necessitates a zero electron current throughout the transistor. Such an assumption, admittedly a good one for the base, would imply the constancy of the quasi-fermi level for electrons in the collector and emitter. To avoid the resulting singularity at the junctions, we have to allow for electron current throughout the transistor or neglect consideration of the collector and emitter regions.

It has been decided, in view of the foregoing, to consider the base region only for the present. A computer program to carry out the numerical integration of Equations (1) through (4), as outlined below, is in preparation.

We assume an impurity distribution in the base. The solution is begun at a still undefined plane $X = 0$ near the emitter-base junction. For want of a better condition, we assume that at this plane the base is exactly space charge neutral. In other words

$$\frac{dE}{dx} = 0$$

Further, we assume that

$$\frac{d^2E}{dx^2} = 0$$

$p(x)$ and $n(x)$ can, then, be obtained numerically for different initial values of p_0 at this plane. The stored majority carrier charge between any two planes $X = X_0$ and $X = X_1$ can be obtained from

$$\int_{X_0}^{X_1} n\,dx = -\frac{J_p}{qD_p}\,pn\,\Big|_{X_0}^{X_1}$$

This equation is a consequence of Equations (1) and (2) with $J_n = 0$.

The electric field is also obtained as a function of X. This process may be stopped when the electric field exceeds a conveniently large value. From qualitative considerations, we expect the solutions to have the nature shown in Fig. 15. For each initial choice of p_0, a family of curves for different values of J_p would be obtained. The minimum in the $p(x)$ curve arises from the product (pE) increasing faster than $\left|\frac{dp}{dx}\right|$. Physically, the minimum of $p(x)$ follows from the following

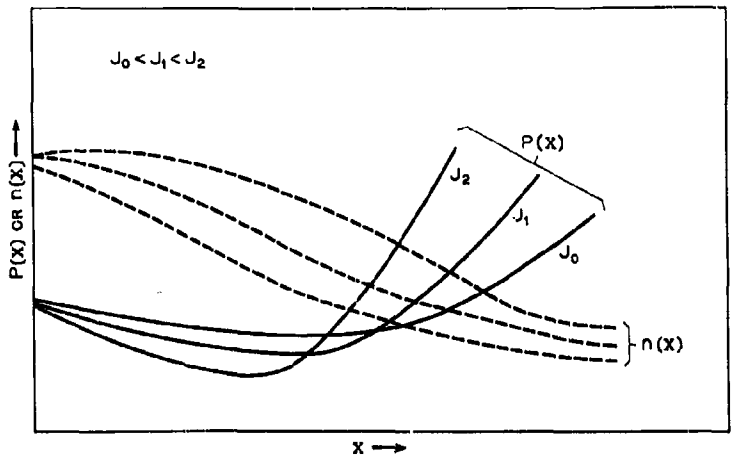

Fig. 15 - Expected qualitative solutions to the charge distribution problem

reasoning. The electric field must change sign near the emitter-base junction. Hence, near the emitter where the electric field passes through zero, the current is entirely carried by diffusion, and $\frac{dp}{dx}$ is negative. The electric field away from this plane increases with X. Thus, the drift component of current increases with X giving rise to a fall in $\left|\frac{dp}{dx}\right|$.

It should be noticed that the solutions to be obtained would not yield the stored charge for a given device. To relate the solutions to a given device, the emitter and collector regions need consideration. This problem, still unsolved, is being actively pursued.

APPENDIX

GENERALIZED EINSTEIN RELATIONSHIP

For low values of electric field, the mobility μ and diffusion coefficient D are related by Einstein's relation

$$\frac{\mu}{D} = e/kT$$

where e is the magnitude of the electronic charge and T is the lattice temperature.

In the presence of moderate or high values of electric field, the electron distribution no longer corresponds to the temperature characteristic of the lattice temperature. The reason for this, of course, is that the electron energy is altered considerably between collisions. This change in the mean energy of the electrons would represent a large change in the effective temperature of the electrons. Thus, the electron distribution is out of temperature equilibrium with the lattice.

In this range of electric fields, the inelastic collisions of the carriers with the acoustical and optical modes of lattice vibrations lead to a first order variation of mobility with the electric field. This variation has been considered by a number of authors (Refs. 6, 7). Their conclusions, well supported by experimental evidence, is that the carrier velocity remains essentially constant at very high electric fields. Thus, the majority carrier current is saturated.

In a reverse-biased collector junction, the electric field is high enough for the carriers to have reached the maximum velocity. The question arises naturally whether the current is limited and whether the current is carried entirely by the electric field. In other words, what is the relationship between mobility and diffusion coefficient in high field regions? Also, can the total current through a region of high electric field be represented as a sum of a drift current and a diffusion current?

To answer these questions satisfactorily, it is necessary to proceed from microscopic considerations only.

We shall consider only the carrier motion along the direction of the electric field.

Let $f(Z, V)\,dV\,dz$ denote the number of carriers with velocities in the range dV in a slab of thickness dz. Under steady-state conditions, Boltzmann's transport equation gives:

$$V_z \frac{\partial f}{\partial z} + \frac{e\epsilon}{m} \frac{\partial f}{\partial V_z} + \frac{f}{\tau(c)} = \int \frac{f(Z, V') F(c \leftarrow c')\, dV'}{\tau(c')} \qquad (1)$$

where

m is the mass of the carriers

V_z is the velocity along the z direction

$c = |V|$ is the speed of the carriers

τ = mean free time, assumed to be dependent only on the speed of the carriers

$F(c \leftarrow c')$ is the collision kernel denoting the probability of transition from speed c' before collision to speed c after collision and

V = components of velocity in the rectangular coordinate system.

The integral on the right hand side represents the carriers scattered into the region under consideration. If the collision kernel is spherically symmetrical, then the integral is a function of c alone. Thus, multiplying throughout by $\tau(c)\, V_z$ and integrating over-all V, this term would vanish because of symmetry.

Thus:

$$\int V_z^2 \tau \frac{\partial f}{\partial z}\, dV + \frac{e\epsilon}{m} \int \tau V_z \frac{\partial f}{\partial V_z}\, dV + \int f V_z\, dV = 0.$$

The same result would follow if $f(z, V')$ is spherically symmetrical and for any $F(c \leftarrow c')$. Thus, in general, for small departure from spherical symmetry of f and/or F, the integral would be approximately zero.

Now

$$e \int f v_z\, dV = J, \text{ the current through the region.}$$

Hence:

$$J = -e \frac{d}{dz} \int V_z^2\, \tau f\, dV - \frac{e^2 \epsilon}{m} \int \tau V_z \frac{\partial f}{\partial V_z}\, dV$$

or, since

$$\tau V_z \frac{\partial f}{\partial V_z} = \frac{\partial}{\partial V_z} (\tau V_z f) - f \frac{\partial}{\partial V_z} (\tau V_z),$$

We have:

$$J = -e \frac{d}{dz} \int V_z^2\, \tau f\, dV + \frac{e^2 \epsilon}{m} \int f \frac{\partial}{\partial V_z} (\tau V_z)\, dV$$

The other term vanishes due to requirements of finiteness. Changing the variables to spherical coordinates defined by:

$$\mu = \cos\theta$$
$$c = |V|$$
$$z = z, \text{ and}$$
$$V_z = \mu c$$

We obtain:

$$J = -2\pi e \frac{d}{dz} \int \mu^2 c^4 \tau f \; dc \; d\mu + \frac{2\pi e^2 \epsilon}{m} \int f c^2 \left(\tau + \mu^2 c \frac{\partial \tau}{\partial c}\right) dc \; d\mu$$

The number of carriers N in the volume under consideration is given by:

$$N = \int f \, dV = 2\pi \int f c^2 \; dc \; d\mu \; .$$

Thus:

$$J = -e \frac{d}{dz} (ND) + |e| \; \epsilon N \mu \tag{3}$$

where

$$D = \frac{\int \mu^2 c^4 \tau f \; dc \; d\mu}{\int f c^2 \, dc \; d\mu} \quad \text{and} \quad \mu = \frac{|e|}{m} \frac{\int f c^2 \left(\tau + \mu^2 c \frac{\partial \tau}{\partial c}\right) dc \, d\mu}{\int f c^2 \, dc \, d\mu}$$

Thus, we find, in general that the current J could be expressed as the sum of two currents—one representing the current carried by the electric field and the other due to the diffusion of carriers.

If D is independent of position, we obtain the usual form for the total current,

$$J = e \epsilon \mu N - e D \frac{dN}{dz}$$

For a distribution function of Maxwellian type:

$$f = A e^{-E/kT_e}$$

where T_e is the effective temperature and E is the energy and for spherical constant energy surfaces, i.e. $E = \frac{1}{2} m c^2$, we obtain:

$$\mu = \frac{|e|}{m} \sqrt{\frac{8}{m^3}} \; \frac{\int_0^\infty e^{-E/kT_e} \; E^{1/2} \left(\tau + \frac{2}{3} E \frac{\partial \tau}{\partial E}\right) dE}{\sqrt{\frac{8}{m^3}} \int_0^\infty e^{-E/kT_e} \; E^{1/2} \, dE}$$

$$D = \frac{2}{3} m \frac{\int_0^\infty e^{-E/kT_e} \tau E^{3/2} dE}{\int_0^\infty e^{-E/kT_e} E^{1/2} dE}$$

If further, the mean free path $\lambda = c\tau$ is independent of energy, we obtain:

$$\mu = +\frac{4}{3} \frac{|e|\lambda}{\sqrt{2\pi m}} \frac{1}{(kT_e)^{1/2}} , \text{ and}$$

$$D = \frac{4}{3} \frac{\lambda}{\sqrt{2\pi m}} (kT_e)^{1/2} , \text{ and}$$

$$\frac{\mu}{D} = |e|/kT_e .$$

Thus, treatment of the high field region of a reverse-biased junction requires that Equation (3) be used.

The equivalent temperature T_e depends on the energy acquired by the carriers between collisions and is thus a function of the electric field. The dependence of T_e on the electric field in low, moderate and high electric field regions has been shown (Ref. 8) to be as follows:

$$\frac{T_e}{T} = \left(1 + \frac{3\pi}{32} \frac{\mu_0^2}{u^2} \epsilon^2\right) \quad \text{in low electric field}$$

$$\frac{T_e}{T} = \left(\frac{3\pi}{32}\right)^{1/2} \frac{\mu_0}{u} \epsilon \quad \text{in moderate electric field}$$

and $$T_e = K\epsilon^2 \quad \text{in high electric field}$$

where μ_0 is the low field mobility, u is the velocity of sound, T is the lattice temperature and K is a constant.

An idea of the numerical magnitude may be obtained by using Shockley's data (Ref. 6):

$$T_e = 550^\circ K$$

$$\mu = 1.5 \times 10^3 \text{ cm}^2/\text{volt sec}$$

$$\epsilon = 4000 \text{ V/cm}$$

For these data, we obtain a diffusion coefficient of 70. This is nearly that which is obtained at low electric fields.

REFERENCES

1. W. Shockley, M. Sparks and G. K. Teal, "The p-n junction transistor," Phys. Rev., Vol. 83, July 1951, pp. 151-162.
2. W. M. Webster, "On the variation of the junction transistor current amplification factor with emitter current," Proc. IRE, Vol. 42, June 1954, pp. 914-920.
3. E. S. Rittner, "Extension of the theory of junction transistor," Phys. Rev., Vol. 94, June 1954, pp. 1161-1171.
4. H. Krömer, "The drift transistor," RCA Laboratories, Princeton, N.J., 1956, p. 202 in "Transistors I".
5. J. M. Early, "P-N-I-P and N-P-I-N junction transistor triodes," B.S.T.J., Vol. 33, May 1954, pp. 517-533.
6. W. Shockley, "Hot electrons in Germanium and Ohm's Law," B.S.T.J., Vol. 30, October, 1951, pp. 990-1034.
7. J. B. Gunn, "Progress in Semiconductors," Heywood and Co., Vol. 2, p. 213.
8. See, for example, R. A. Smith, "Semiconductors," Cambridge University Press, 1959, Chapter 5.

Chapter 4

AVALANCHE MULTIPLICATION IN GERMANIUM PNP DIFFUSED-BASE TRANSISTORS*

By A. B. Kuper

4.1 INTRODUCTION

Development of high power diffused-base germanium transistors (DBGT) has been impeded by the inability to realize the breakdown voltages which should be obtained for the collector resistivity selected. Surface breakdown has frequently been invoked to explain this observation. To obtain a better understanding of the cause of the low breakdowns, a study of avalanche multiplication in PNP germanium diffused-base transistors with lightly doped collectors has been made and is reported herein.

S. L. Miller (Ref. 1) observed that the collector characteristics of alloy transistors at constant emitter current approximately fit a multiplication expression:

$$M = 1/[1 - (V/V_B)^n] \qquad (1)$$

where

M = multiplication

V_B = collector breakdown voltage

V = collector-base applied bias

n = a constant, ~ 3 for holes

although he did not correct for base width narrowing effects. He then assumed Equation (1) was correct and used measurements of floating base breakdown on many transistors with the same base doping but different current gains and breakdown voltages to determine n. This two-terminal breakdown method included surface currents. However, from the interpretation of the data, the contribution from surface breakdown was shown to be small in those transistors.

In the present work collector characteristics due to holes injected into the collector junction under the emitter are measured at constant I_E. Surface currents

*The work reported here was not done under this contract, but is included because of its relevance.

are measured separately. This is possible because the emitter injects carriers into the collector junction a sufficient distance from the free surface of the collector in the DBGT so that one may separate body and surface current by a three-terminal measurement. The method takes base width changes into account and requires no *a priori* assumption of $M(V)$.

It is found that Equation (1) is closely fitted by our data, that $n \cong 3$ as Miller reported, and that body breakdown (V_B) is low in DBGT. The principal cause of the low V_B observed with 2 ohm-cm P-type collector starting material appears to be copper contamination. Careful measurement of collector capacitance indicates an added barrier fixed charge density of 10^{15} which corresponds to copper saturation of 3×10^{14} at the base diffusion temperature. Taking this into account, values of V_B obtained in the present work in the neighborhood of 1.5 ohm-cm P-type collector resistivity are approximately 15 per cent lower than those reported by Miller.

This V_B which should be used in using Equation (1) for purposes of transistor design is found to be about 18 per cent larger than that conventionally measured on an oscilloscope.

4.2 METHOD OF MEASUREMENT

In a three-terminal measurement of body multiplication the preferred method is to maintain emitter current (I_E) constant. Then, as the reverse collector-base voltage (V) is increased, the injected collector current (I'_C) is independent of the base narrowing which results from collector barrier widening (Ref. 2). The following designations will be used.

Unprimed currents are total currents.

Primed are those resulting from forward-biasing the emitter.

Doubled primed are those currents measured in the experiment.

Superscript R designates currents which flow when the emitter is reverse-biased.

The observed injected collector current (I''_C) will increase for fixed emitter current not only because of multiplication but also because of a decrease in injected base current (I'_B). I'_B will decrease in general as the collector-base voltage is increased for two reasons: (1) V_{EB} is decreasing and (2) the base width is decreasing. In the diffused base transistor, I'_B is independent of base width, as will be shown experimentally, because base recombination is negligible. Thus, we need to consider only I'_B (V_{EB}), which we can measure.

The method is shown schematically in Fig. 16. At a fixed value of V_{CB}, the emitter is first reverse-biased so that no current is injected into the collector. In Fig. 16(a) are shown the currents which flow. These currents will contain surface, space charge recombination, and internal field emission current, and are subtracted from the body currents measured in the following steps.

At the same value of V_{CB}, the emitter is next forward-biased to a constant I_E as shown in Fig. 16(b) and the collector current, I''_C, due to injection and

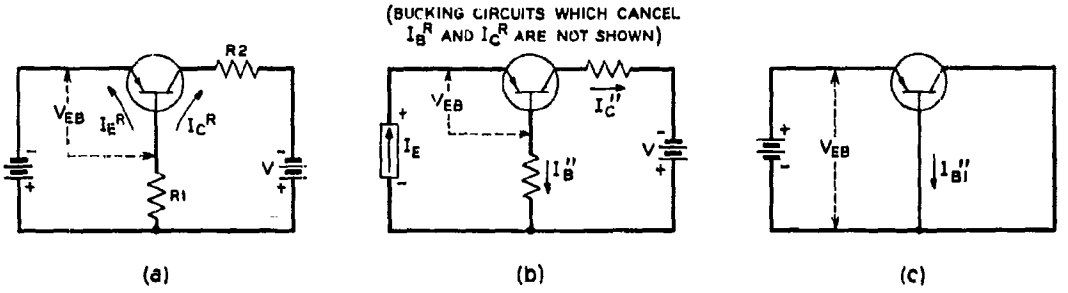

Fig. 16 - Experimental method. (a) Both junctions reverse biased. (b) After bucking the currents shown in (a), emitter is forward biased with V unchanged. (c) Circuit to obtain the base current due to forward emitter bias when M = 1

collector multiplication is measured. The emitter-base voltage required to maintain I_E is also measured.

In order to know how much of the increase in I''_C is due to collector multiplication as V_{CB} is increased, one needs to measure the base current as a function of V_{EB} separately, with $M = 1$. This may be done at $V_{CB} = 0$ as shown in Fig. 16(c) where the observed base current is designated, $I''_B(M=1) = I''_{B1}$. Thus we have $I''_C(V_{CB})$ and $I''_{B1}(V_{CB})$. Multiplication at a particular collector-to-base voltage can now be calculated from the equation

$$M = I''_C/(I_E - I''_{B1}) . \qquad (2)$$

4.3 EXPERIMENT

The experiment consisted of measurements of dc transistor currents as a function of junction biases. Batteries were used to supply the necessary voltages. The emitter supply could be switched from a fixed reverse to a variable forward bias. Emitter current and collector voltage were measured with a meter accurate to 1/2 per cent of full scale. Emitter-base voltage was measured to five significant figures using a slide-wire potentiometer. Collector and base currents were measured with an accuracy of 2 per cent using calibrated dc amplifiers and digital voltmeters. Circuits were provided to balance out the measurement of the base and collector currents flowing when the emitter was reversed. To assure that bucking remained constant during measurement, the transistor was clamped to a brass block whose temperature was maintained at 30° C ± 0.1° C. The power dissipated within the device was kept low so that internal temperature rise would be insignificant.

The experimental procedure was as follows. The collector and emitter diodes were reverse-biased at fixed values of V_{CB} and V_{EB}; and the collector current was balanced to zero by offsetting the zero of the measuring instrument. The emitter was then forward-biased to inject current I_E. Collector current and V_{EB} were then measured for each value of V_{CB} up to that at which the collector current had approximately doubled ($M = 2$). The collector was then connected to the base and the base current measured as a function of V_{EB}. The previous V_{EB} data could then be used to obtain the base current, I''_{B1}, which would be observed in the absence of multiplication. M was then calculated from Equation (2).

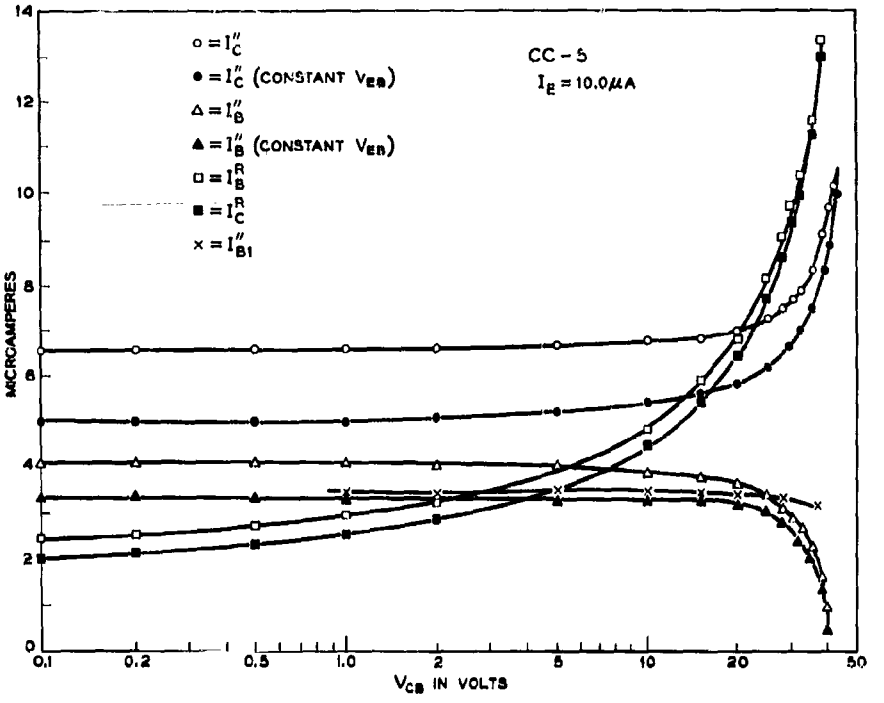

Fig. 17 - Experimental data for one conventional PNP diffused-base Ge transistor with 2 ohm-cm P-type collector starting resistivity (I_E = 10 μa refers to I''_C and I''_B.)

In Fig. 17 are shown data for one conventional PNP DBGT which has a nearly step collector junction with a nominal 2 ohm-cm P-type collector region. In addition to the currents I''_C and I''_{B_1} measured with I_E = 10.0 μa, the currents I^R_B and I^R_C which are measured with the emitter reversed are also shown. These currents would give a spurious collector characteristic if a two-terminal measurement were made of this collector junction. I''_B is the base current observed after bucking. Note that at 1 volt, $I''_{B_1} + I''_C = 3.46 + 6.60 = 10.06$ μa. All data checked in this way to within 3 per cent at low collector voltage. A 1 per cent correction to make $M = 1.00$ = constant at low collector voltage represents approximately a 1 per cent change in V_B and a 5 per cent change in n.

Also shown in Fig. 17 are I''_C and I''_B vs. collector voltage when V_{EB} = constant. Two things should be noted: (1) I''_B (V_{EB} = constant) = constant until $M > 1$, i.e. the base current is independent of base width and (2) I''_C (V_{EB} = constant) is base width dependent.

In Fig. 18 are data at I_B = 55.0 μa for the same transistor. The multiplication is independent of I_E at these current levels as can be seen by comparing Figs. 17 and 18.

The data of Fig. 17 when put into Equation (2) give $M = 1.015$ for $V < 10$ volts. Since M is observed to be constant, it is assumed $M = 1.000$ at low voltage, the deviation being due to systematic error. If all M are divided by 1.015, the result is shown in Fig. 19. The correction has negligible effect for $M > 1.05$ above which point Equation (1) is seen to hold.

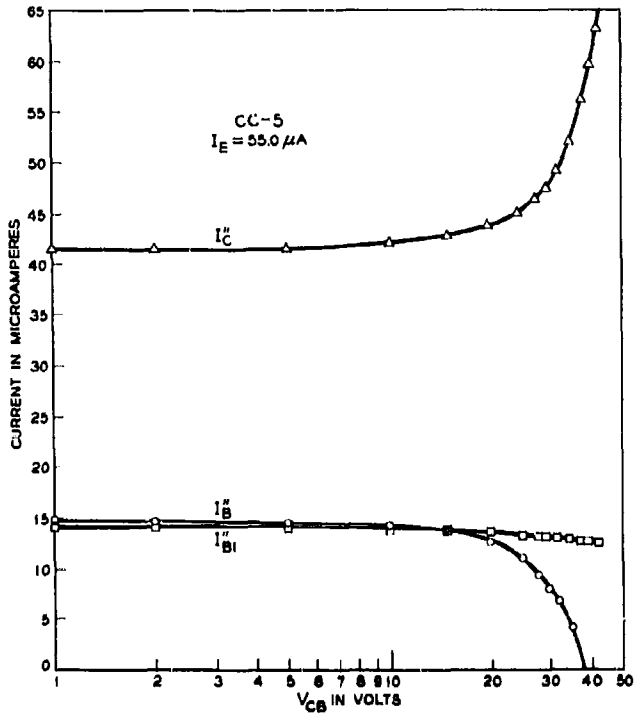

Fig. 18 - Experimental data at higher I_E for transistor of Fig. 17

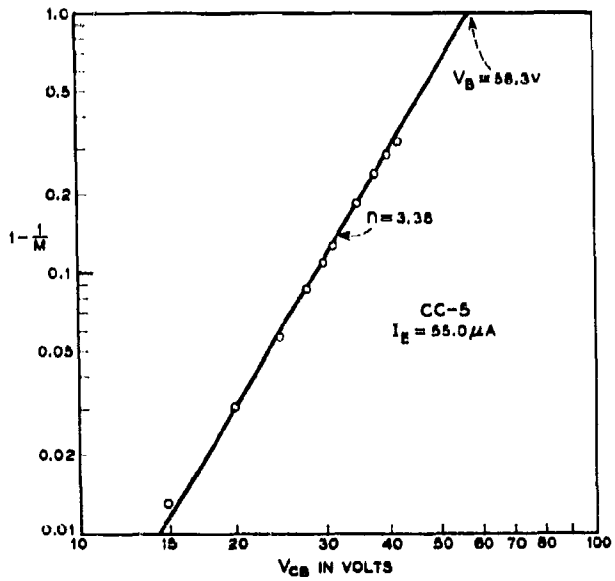

Fig. 19 - Multiplication due to injected holes

TABLE 4-1

Transistor	V_B	n	Correction	First Point	BV_{CBO} (1 ma)	BV_{CBO} (5 ma)	$\frac{V_B}{BV_{CBO}(1\ ma)}$	Starting ρ_p (ohm-cm)	Junction $\lvert N_D-N_A \rvert$ ($\times 10^{-15}$)
CE-9	58.0 v	3.32	1.02	15 v	49.2 v	51.2 v	1.18	1.96	3.0
CC-5	58.3	3.38	1.015	15	49.4	51.0	1.18	2.1	
CJ-14	62.0	3.37	1.019	10	52.3	54.4	1.19	2.0	
CC-11	56.5	3.08	1.02	15	47.0	48.7	1.20	2.1	
CC-12	55.7	2.96	1.03	15	46.2	47.6	1.20		
CE-22	59.0	3.41	1.02	20	50.9	52.6	1.16	2.26	3.0
CG-18								1.81	2.9
CI-20								2.16	2.5
2105	51.0	3.04	1.03	17	43.6		1.17	1.0	~ 3.5
CK-23 (EPI)	~ 200	3 to 4	1.01	50	100.0				0.5
24-12 (PNP Alloy)	158.0	3.36	1.011	30	119.0		1.33	3.0	0.8

Results of this type are given in Table 4-1. It is noted that V_B, the breakdown obtained by extrapolation to $M = \infty$, is a good number as shown by the 1:1 correspondence between V_B and the breakdown obtained using the test circuit with emitter open. V_B from Table 4-1 are compared to published data (Refs. 1, 4) in Fig. 2(c).

Resistivities given in Table 4-1 are measured starting values for the first eight transistors (2 ohm-cm P-type). Doping obtained from collector capacitance per unit area is given in the last column and is seen to be about 1×10^{15} cm^{-3} more than is expected from the starting resistivity.

The 2105 transistor, a conventional DBGT with a nominal starting 1 ohm-cm P-type collector was measured as a check on the method. It confirmed the oscilloscope observation that breakdown voltage was about 20 per cent lower in 1 ohm-cm as compared to 2 ohm-cm P-type. Collector capacity gave approximately the starting doping.

The PNP alloy transistor was measured to verify the high V_B measured by other methods. It was a unit which was selected because the collector barrier did not reach through to the emitter before breakdown. Although the experimental method is not intended for alloy transistors, M may be obtained to a good approximation since the base current of interest is not a strong function of V. This can be seen experimentally when $M = 1$ since $I''_{B1}\ (V = 0) \cong I''_B\ (V = 25$ volts). $V_B = 158$ volts is in satisfactory agreement with Miller's results for a junction with 8×10^{14} cm^{-3} fixed charge in the barrier as determined from capacity.

A transistor of the same geometry as CC-5 but made with a collector region consisting of 13 microns of lightly doped epitaxial Ge deposited on a degenerate seed is CK-23 in Table 4-1. Collector capacity gives the barrier charge equal to 5×10^{14} cm^{-3} and shows the collector barrier sweeps out the high resistivity region at 35 volts. Above this voltage the electric field in the barrier rises faster than in a simple step junction. Nevertheless, it was found that $M \approx 1.02$ at 70 volts which suggested a $V_B \approx 200$ volts for $3 < n < 4$ in a thick layer of this material.

4.4 DISCUSSION

The low breakdown observed in diffused germanium transistors which use 2 ohm-cm P-type starting collector material appears to be due mainly to an increase during processing of the fixed-charge concentration in the collector barrier. Copper introduced during diffusion may be present in the final device at a concentration of 2 to $3 \cdot 10^{14}$ cm^{-3}. Triply ionized copper could then increase the ionized acceptor concentration within the collector barrier by as much as $9 \cdot 10^{14}$ cm^{-3}. Starting with 2 ohm-cm collector resistivity with a gallium concentration of $1.8 \cdot 10^{15}$ cm^{-3}, junction capacitance/area would give as much as $2.7 \cdot 10^{15}$ cm^{-3} in approximate agreement with the data in the last column of Table 4-1. Taking the doping change into account, V_B is approximately 15 per cent below Miller's value as shown in Fig. 20.

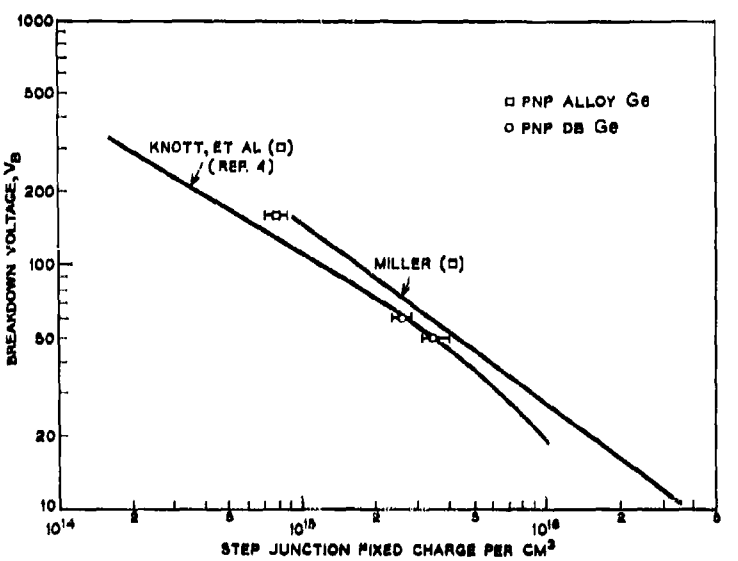

Fig. 20 - V_B results from present method compared to published BV_{CBO} on indium alloy transistors

The fact that body avalanche multiplication measured under the DBGT emitter in the present work is somewhat higher than that found on PNP alloy transistors with the same collector barrier doping might be due to high multiplication in localized areas of the junction. However, examination of the collector current shows no

microplasma noise throughout the range of the measurements. High multiplication occurring essentially homogeneously over the junction might be due to a uniform distribution of defects or impurities which result in decrease in the energy required for electron-hole pair production in the collector barrier. This might arise in a particular device from processing steps such as polishing, heat treatments, or alloying.

For purposes of calculation (Ref. 3) it is desirable to know the parameters to be used in Equation (1). The present work gives:

$$n = 3.2 \pm 0.2 \tag{3}$$

for holes injected into a step barrier extending into P-type germanium with $N_A \cong 2$ to 4×10^{15} cm^{-3} . This is in agreement with values given by Miller. The value of V_B, it appears, must be measured for the particular type of transistor one is using. If one makes the usual collector diode measurement, one measures a breakdown voltage which is dependent on surface breakdown and, in any case, is not the desired value at $M = \infty$. Empirically, for DBGT's given in Table 4-1, a good approximation to the desired V_B is:

$$V_B = 1.18\ BV_{CBO}\ (I_C = 1\ \text{ma}). \tag{4}$$

REFERENCES

1. S. L. Miller, Phys. Rev. 99, 1955, p. 1234.
2. J. M. Early, Proc. IRE 40, 1952, p. 1401.
3. J. M. Early, IRE Trans. ED-6, 1959, p. 322.
4. R. D. Knott, I. D. Colson, M. R. P. Young, Proc. Phys. Soc. (London) B68, 1955, p. 182.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Chapter 5

STATUS OF INTEGRATED CIRCUITS AND FUNCTIONAL DEVICES

By R. Lindner, K. E. Martersteck, Jr., and J. H. Forster

5.1 INTRODUCTION

During this quarter work has continued in several areas. The fabrication and evaluation of multiple-chip integrated circuits, development of exploratory techniques for fabrication of these circuits and design of components used in these circuits have been continued.

The work on the multiple chips has included completion of the first-order performance evaluation of the LLL gates incorporating diffused-silicon resistor chips discussed in the previous report (Ref. 1). The previous report presented data on dc input margins, turn-on and turn-off times, and crosstalk for a pair of two-diode input gates incorporated in a single package. During this quarter, the propagation delay per stage for similar LLL gates has been determined as a function of operating temperature, for fan-out of one and three. These delay times are found to be about five and six nanoseconds, respectively, and vary only slightly with temperature. Details of the measurements are presented below.

Exploratory work on the integration of film resistors is also being carried out. This work includes the evaluation of suitable substrates for the film components, investigation of techniques for interconnection with semiconductor devices, and consideration of package modifications.

Finally, the function of the multi-junction level shifter diode in the LLL, NAND gate configuration has been reviewed. Although the requirements on the level shifter have been considered previously (Ref. 2), the use of newer components (planar) diodes and planar epitaxial transistors) in the chip circuits make this review necessary. In particular, it has been shown that with an epitaxial 2N914 transistor, a two-junction level shifter provides essentially the same dc input margins as a three-junction shifter working into a nonepitaxial transistor. The stored charge requirement on the level shifter and the turn-off time for the gate are also reduced when the epitaxial transistor is used. Measurements of dc characteristics for one-, two- and three-junction level shifters at operating temperatures from

room temperature to 80° C are discussed below. In addition, stored charge and switching time measurements for the 2N914 epitaxial transistor are included.

5.2 PROPAGATION DELAY MEASUREMENTS

The integration of a pair of two-input LLL gates (including diffused-silicon resistors) in a single 9-pin header has been discussed (Ref. 1). The package layout and schematic are shown in Fig. 21. Further tests have been conducted during this quarter to check the circuit operating characteristics. The most significant of these, the propagation delay time, has been measured using the circuit arrangement indicated in Fig. 22. The dotted lines indicate gates in the same package. The first

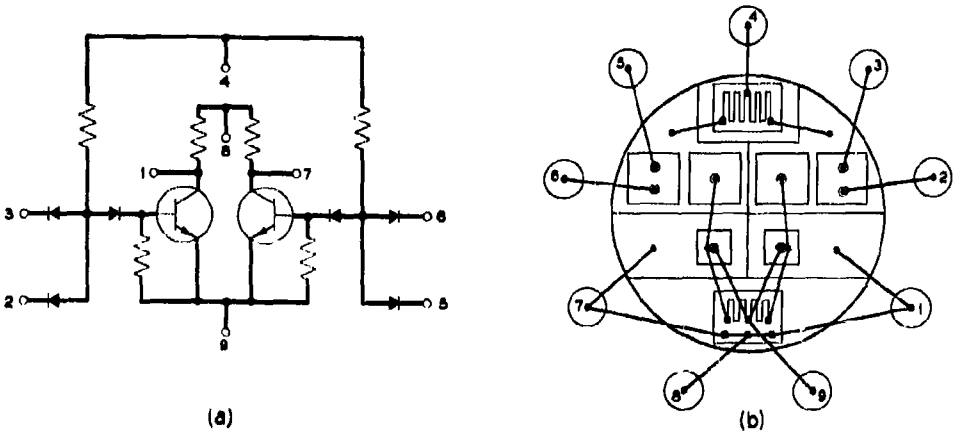

Fig. 21 - Schematic and package layout for double LLL gate

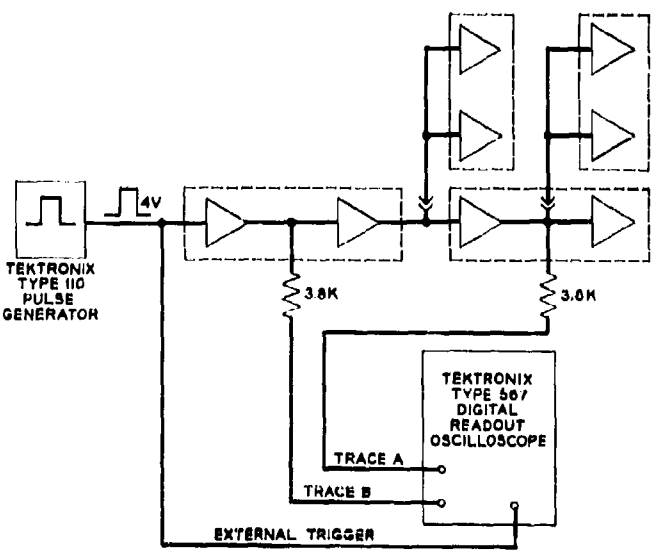

Fig. 22 - Propagation delay time measurement circuit

Table 5-1

PROPAGATION DELAY TIMES FOR INTEGRATED LLL GATES

Temperature	Propagation Delay Per Stage, t_D
-60°C	6.0 ns
-40°C	5.6 ns
-20°C	5.2 ns
0°C	5.5 ns
20°C	5.5 ns
40°C	5.5 ns
60°C	5.9 ns
80°C	6.1 ns
100°C	6.5 ns

gate acts as a driver to provide a pulse to the following stages. The time (Δt) between the midpoint voltage shifts at the second gate input and the third gate output are measured on an oscilloscope, and the propagation delay per stage (t_D) is defined as $\Delta t/2$. For gates with fan-out of one, t_D is about 5.5 ns, and for gates with fan-out of three, t_D is about 6.3 ns. For the integrated gates, t_D varies only slightly with temperature. Typical results for t_D as a function of temperature for a fan-out of one are tabulated in Table 5-1.

These values of t_D are typical for the integrated LLL gates incorporating silicon resistors. However, it should be pointed out that in actual systems use, where output pulses may need to be transmitted appreciable distances, parasitic elements must be minimized to ensure similar average propagation delay times.

5.3 LEVEL SHIFTER MEASUREMENTS

Economies may often be achieved without loss in performance by simplification of the circuit or its components. Thus, simplification of the integrated LLL gates (Fig. 21) has been achieved by the combining of two resistors on one chip, with negligible loss in performance. The use of a single- or double-junction level shifter in place of the triple-junction unit often used represents a further desirable simplification.

Accordingly, an experimental investigation of the dc margins for the LLL gate comprised of planar computer diode inputs, single-, double- or triple-junction level shifters, and a planar epitaxial (2N914) output transistor has been made. In

addition, the stored charge and switching times for several 2N914 transistors have been measured. The experimental results, outlined below, indicate that the improved performance of the epitaxial transistor does permit substantial simplification of the level shifter design.

5.3.1 DC Margin Measurements

Referring to the LLL, NAND gate of Fig. 23, if all the voltages on the input diodes are high, current is directed through the level shifter into the base of the transistor, which saturates and provides a low voltage at the output. On the other hand, if one of the input voltages is low, current is directed away from the point A through the low input. The voltage at A is however, not zero, but the sum of the input voltage and the drop across the input computer diode. The primary function of the level shifter is to prevent the voltage at A from continuing to maintain the saturation base drive for the output transistor.

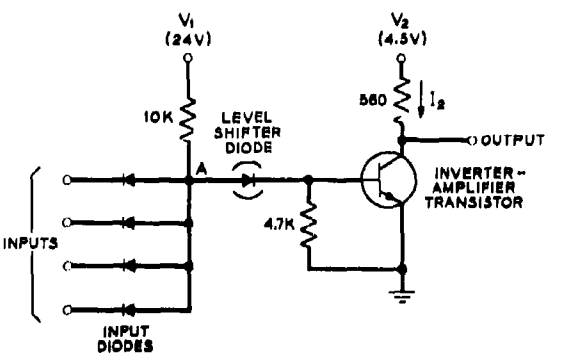

Fig. 23 - Low-level logic gate

The input voltage plus the computer diode drop must be greater than the sum of the voltage drop across the level shifter and the base-emitter drop of the output transistor in the on state, if base drive is to be sufficient to turn on and maintain the output transistor in saturation. To evaluate dc margin requirements, the input voltage required (V_{in}^*) to drop the output transistor collector 0.5 volts from its normal high value of 4.5 volts is calculated from measurements of computer diode, level shifter, and transistor voltage drops. This value of V_{in}^* may then be compared with the input driving transistor V_{CE} to determine input margins.

For the circuit of Fig. 24,

$$V_{in}^* = V_{BE} + V_{LS}(I_{LS}) - V_{CD}(I_{CD}) \qquad (1)$$

where

V_{BE} = base emitter voltage for an output voltage (V_{out}) of 4.0 volts

I_{LS} = base current required for V_{out} = 4.0 volts

V_{LS} = voltage across level shifter for a forward current of I_{LS}

V_{CD} = voltage across computer diode for a forward current of I_{CD}.

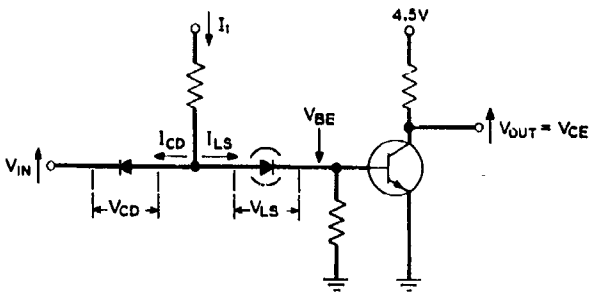

Fig. 24 - DC voltages and currents in an LLL gate

I_{LS} and V_{BE} have been determined experimentally as functions of temperature for several transistors, as indicated by the circles in Figs. 25(a) and 25(b). V_{LS} can be read off experimentally determined I-V characteristics for level shifters once I_{LS} is determined, and V_{CD} may be determined from measured average computer diode characteristics.

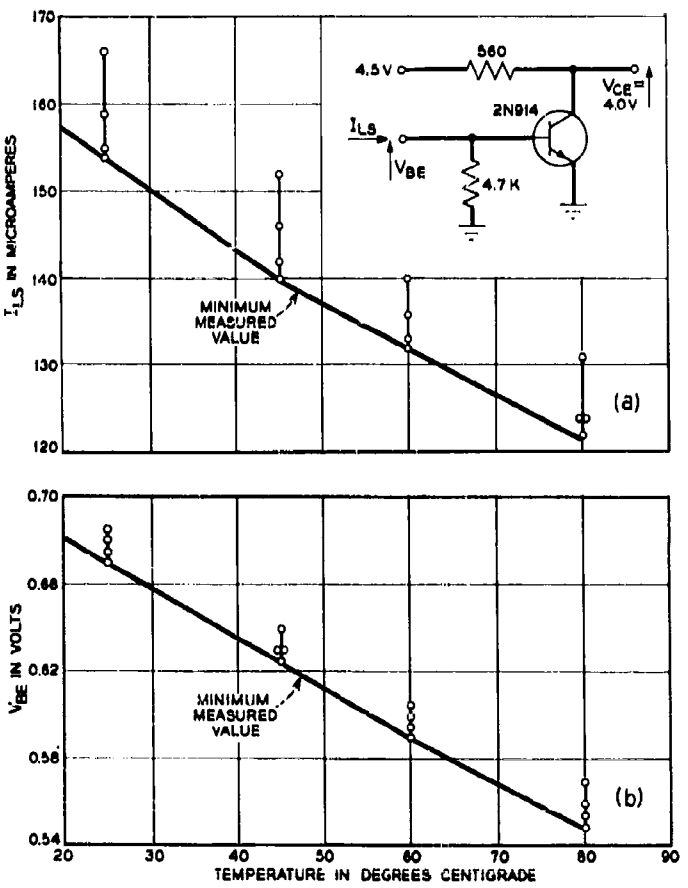

Fig. 25 - I_{LS} and V_{BE} for V_{CE} = 4 volts

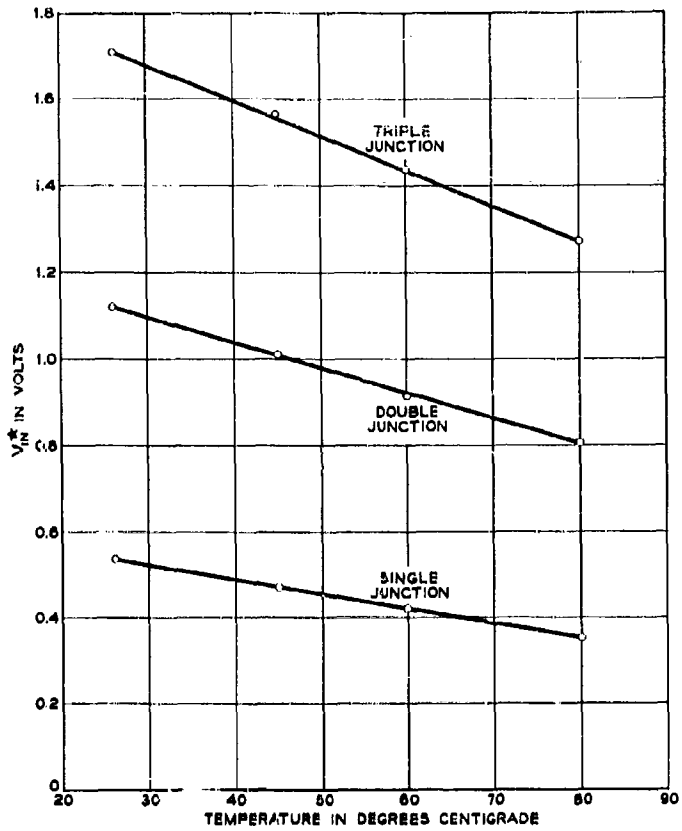

Fig. 26 - V_{in}^* for LLL gate using single-, double-, or triple-junction level shifter

These operations have been performed, and V_{in}^* has been computed from Equation (1) assuming a pessimistic value of I_1 = 3 ma. The results are summarized in Fig. 26, where V_{in}^* is plotted as a function of temperature for single-, double-, and triple-junction level shifters.

The dc input margin depends on the saturation voltage of the transistor driving the gate input. For the 2N914 epitaxial transistor, the saturation voltage (I_b = 1 ma, I_C = 30 ma) is 0.25 volts or less and essentially independent of temperature. It can be seen from Fig. 26 that a single-junction level shifter provides some dc margin even at 80° C. However, if substantial input noise protection is desired, a double-junction level shifter is necessary. A triple-junction shifter is probably not necessary except for special situations. It is worth noting that the input margin offered by the double-junction shifter used with an epitaxial transistor is almost as great as that for a triple-junction shifter – nonepitaxial transistor combination.

Finally, it should be pointed out that decreasing the number of level shifter junctions decreases the voltage required to keep the output transistor in the on state, and therefore improves the dc margin for the input off condition.

5.3.2 Charge Measurements

Another requirement on the level shifter performance in the gate of Fig. 23 is that during a switching transient the impedance of the level shifter must remain low while the transistor is being turned off. This allows a greater reverse base drive and hence faster switching. This requirement is satisfied if the charge stored in the level shifter is substantially greater than the charge stored in the output transistor.

The stored charge measured for epitaxial transistors is substantially less than for nonepitaxials, as indicated in Fig. 27, which compares stored charge as a function of collector current for a 2N560 and several 2N914 transistors. In Fig. 28, the measured stored-charge forward-current characteristics for two types of level shifter is indicated. Curve I is for a triple-junction level shifter satisfactory for use with a transistor like the 2N560, and Curve II is for a single-junction shifter, for use with a 2N914.

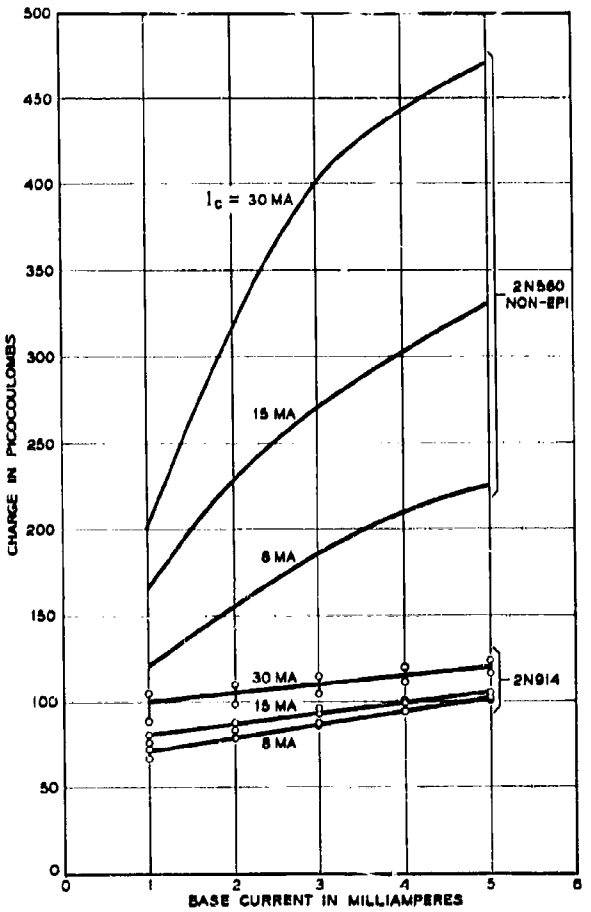

Fig. 27 - Stored charge as a function of base current and collector current for epitaxial (2N914) and non-epitaxial (2N914) transistors

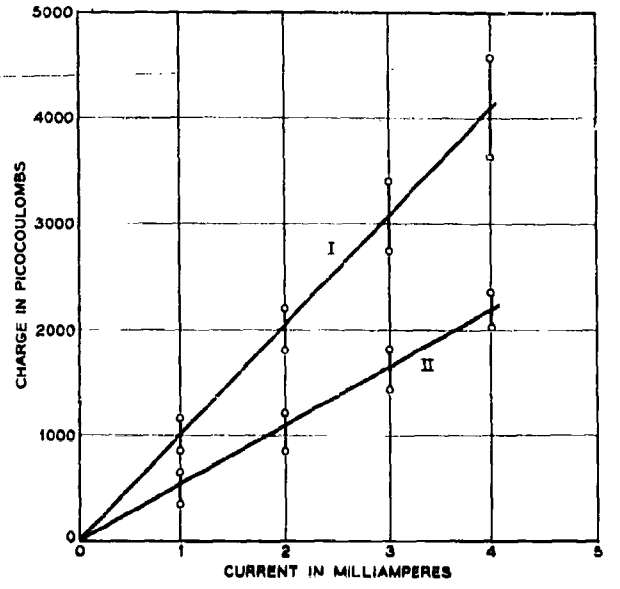

Fig. 28 - Stored charge as a function of current for level shifter diodes

The charge stored in a level shifter diode is a function of the minority carrier lifetime near the p-n junction. The lifetime is in turn dependent on recombination centers introduced during the processing of the device. Special processing techniques are required to produce the long lifetime and relatively large stored charge associated with devices like those represented by Curve I, whereas production of devices with characteristics like those of Curve II can be produced with more conventional techniques.

Thus, the use of the epitaxial transistor in the LLL gate substantially reduces the stored-charge requirement for the level shifter, and simplifies its fabrication.

5.3.3 Switching Time Measurements

The switching times of LLL gates with single- and double-junction level shifters have been measured over the temperature range from 25 to 80° C. As might be expected, the turn-on times for both kinds of shifter are similar (about seven nanoseconds) but the turn-off time is slightly shorter with the double-junction shifter (20 ns as compared to 24 ns). Temperature dependence of turn-on and turn-off times is small.

5.4 CONCLUSIONS

Propagation delay per stage has been determined for integrated LLL gates using silicon resistor chips. Values of several nanoseconds are obtained at operating temperatures from -60° C to +100° C.

With planar epitaxial transistors a two-junction level shifter provides almost the same input margin as a three-junction level shifter, nonepitaxial combination. The epitaxial transistor also permits a reduction in stored charge required for the level shifter, a factor leading to simpler device processing.

Reduction in the number of level shifter junctions results in an almost negligible loss in turn-off speed.

REFERENCES

1. K. E. Martersteck and J. H. Forster, "Engineering Services on Transistors," Report No. 9, Contract DA 36-039 sc-89201, 1 November 1962.

2. S. F. Sampson, personal communication.

SECTION 5 - CONCLUSIONS

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Control of fabrication processes for the 0.25 watt, 1 Gc transistor has been improved. Units now have lower power gain at 1 Gc than ones previously made. A systematic investigation of the cause must be carried out so that the performance may be improved.

The evaporated oxides used for planar structures have pin holes and low breakdown after heat treatment. Refined evaporation techniques and cleaning procedures must be established to improve them. The use of thermally deposited oxides and photolithographic techniques for control of surface geometries appear to offer advantages over evaporated oxides. The feasibility of their use in the microwave transistors should be investigated.

Epitaxial germanium still does not consistently sustain the same breakdown field and offer the same resistance to burnout as bulk germanium. Improvements in material are still needed.

Improvement in metalizing of beryllia parts for the power coaxial header is also required before bond strengths equivalent to those obtained with other ceramics are obtained.

The base resistance in the equivalent circuit of microwave power transistors should be represented by a complex impedance due to the distributed nature of the bypassing effect of the forward-biased emitter junction and the feedback of the collector-junction capacitance.

In the design of diffused-base transistors with lightly doped collector barriers (i.e. over 1 ohm-cm) published data on breakdown voltage should not be used to compute avalanche multiplication. Higher multiplication has been found in devices with lightly doped collector barrier regions. The multiplication is not a surface effect or due to microplasmas, but appears to be a true multiplication of injected current.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Input margins for LLL gates using single-, double-, or triple-junction level shifter diodes and 2N914 transistors have been established. Use of the 2N914 improves dc margins substantially, and reduces the stored-charge requirement on the level shifter.

Propagation delay times have been determined for the integrated two-diode input gates described in the previous report, which incorporate diffused-silicon resistors. Delay per stage is about 6 ns, and varies only slightly with temperature.

SECTION 6 - PROGRAM FOR THE NEXT INTERVAL

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

During the next quarter the following will be stressed:

1. A systematic study of the low gain problem in the 0.25 watt transistors, and improvement of gain.

2. Continuation of model fabrication to maintain the facility for consistent processing.

3. Refinement of techniques for depositing oxides and electrodes.

4. Investigation of photolithographic techniques for making the proposed planar structures.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Exploratory work on the integration of silicon or film resistors with semiconductor chips will be continued.

Development and design of semiconductor chips for integrated circuits will continue.

SECTION 7 - IDENTIFICATION OF PERSONNEL

The following key technical personnel have contributed substantially to the work reported for this contract period:

JOHN H. FORSTER

B.A. 1944, M.A. 1946, University of British Columbia; Ph.D. 1953, Purdue University; Bell Laboratories 1953. Since joining the Laboratories, Dr. Forster has been engaged in research on semiconductor devices including point-contact transistors, transistor reliability and surface studies, and development of low-noise alloy transistors. More recently he has been engaged in development of junction diodes for microwave applications. He also served as instructor of semiconductor electronics in the Laboratories Communications Development Training program. At present he is engaged in the development of functional devices and integrated circuits. He is a member of Sigma Pi Sigma and Sigma Xi.

J. KOCSIS

J. Kocsis received his B.Sc. in Electronics at the Technical University of Budapest, Hungary in 1953, and his Ph.D. at the University of London, England in 1962. Prior to his research work for his Ph.D. degree, Mr. Kocsis worked for three years on the design of television video monitors and aerial systems. In London, England he worked on characterization of semiconductor devices, measurement techniques, designing and building equipments for measuring transistor parameters.

Since joining Bell Laboratories in July 1962, Mr. Kocsis has been working on the design and characterization of microwave transistors.

ALAN B. KUPER

Alan B. Kuper received his B.S. in Physics from the University of Chicago in 1949 and his Ph.D. in Physics from the University of Illinois in 1955. His work in experimental metal physics was continued at Princeton University before coming to Bell Telephone Laboratories in 1957. Since then he has been engaged in diffusion, alloying and materials studies connected with diffused-base germanium transistor development. He was in the Navy from 1943 to 1946 and is a member of the American Physical Society.

R. LINDNER

R. Lindner graduated Cooper Union in June 1953 with a B.M.E. degree and obtained a Master's Degree in mechanical engineering from M.I.T. in June 1954. He joined the Laboratories in June 1954, after two summers of previous employment. He graduated from Communications Development Training program in June 1957, and is presently working on solid state device development.

KARL E. MARTERSTECK

Karl E. Martersteck graduated from the University of Notre Dame in 1956 with a Bachelor's Degree in Physics. Upon graduation he was commissioned in the U.S. Navy and served as engineer aboard a destroyer for three years.

He joined Bell Telephone Laboratories in 1959 and received a Master's Degree in Electrical Engineering from New York University in 1961 through the Communications Development Training Program. Mr. Martersteck is currently engaged in the development of semiconductor devices and integrated circuits.

JAMES T. NELSON

James T. Nelson received his B.A. degree from Reed College in 1950. In 1952 he received his M.A. and in 1955 his Ph.D. from the University of Oregon. At the University of Oregon he worked as a research fellow on the development of a scintillation counter for the detection of soft x-rays and an investigation of the electrical and optical properties of intermetallic compounds.

Mr. Nelson became a member of the Laboratories in 1955 and has been working on the development of a silicon power transistor and germanium diffused-base transistors.

T. B. RAMACHANDRAN

T. B. Ramachandran received his Ph.D. in 1961 from Lehigh University, where he is a research associate in Electrical Engineering. He has been on temporary assignment at Bell Telephone Laboratories.

DISTRIBUTION LIST

10 copies to: Commander, Armed Services Technical Information Agency, Arlington Hall Station, Arlington 12, Virginia
ATTN: TISIA-21

3 copies to: USCONARC Liaison Officer, U.S. Army Electronics Research & Development Laboratory, Fort Monmouth, New Jersey

3 copies to: Commanding Officer, U.S. Army Electronics Command, Fort Monmouth, New Jersey
ATTN: AMSEL-AD

2 copies to: Advisory Group on Electron Devices, 346 Broadway, 8th Floor, New York 13, N. Y.

2 copies to: Chief, U.S. Army Security Agency, Arlington Hall Station, Arlington 12, Virginia

Commanding Officer, U.S. Army Electronics Research & Development Laboratory, Fort Monmouth, New Jersey

1 copy to: ATTN: Director of Research/Engineering
3 copies to: ATTN: Technical Information Center
1 copy to: ATTN: Technical Documents Center
1 copy to: ATTN: Ch, S&M Br., Solid State & Frequency Control Division
1 copy to: ATTN: Ch, M&QE Br., Solid State & Frequency Control Division
1 copy to: ATTN: Ch, Radar Equipment Branch
1 copy to: ATTN: Dir, Astro-Electronics Division
1 copy to: ATTN: Systems Engr Division
1 copy to: ATTN: Director, Met Division
1 copy to: ATTN: Director, Countermeasures Division
1 copy to: ATTN: Director, Applied Physics
1 copy to: ATTN: Director, Transmission Facilities
1 copy to: ATTN: Director, Surveillance Department
1 copy to: ATTN: Director, Electronic Components Department
1 copy to: ATTN: Director, Exploratory Research Division "E"
2 copies to: ATTN: Director, EP&M Division
1 copy to: ATTN: Director, Power Sources Division
2 copies to: ATTN: Director, Communications Department
1 copy to: ATTN: Director, Solid State & Frequency Control Division
1 copy to: ATTN: Dept Dir, Solid State & Frequency Control Division
1 copy to: ATTN: Mr. Matthei, Solid State & Frequency Control Division
1 copy to: ATTN: Mr. Brand, Solid State & Frequency Control Division
1 copy to: ATTN: Mr. Hambleton, Solid State & Frequency Control Division
1 copy to: ATTN: Rpts Distribution Unit, Solid State & Frequency Control Div. (Record Copy)
1 copy to: ATTN: Mr. Ahlstrom, Solid State & Frequency Control Division
1 copy to: ATTN: Mr. Armata, Solid State & Frequency Control Division
3 copies to: ATTN: Dr. Meindl, Solid State & Frequency Control Division
6 copies to: ATTN: Dr. Wandinger, Solid State & Frequency Control Division

Director, U.S. Naval Research Laboratory, Washington 25, D.C.

1 copy to: ATTN: Code 2027
ATTN: Code 1071
ATTN: Code 6451
ATTN: Code 4133
ATTN: Code 5210

1 copy to each of the following:

Commander, Air Force Cambridge Research Laboratory,
Laurence G. Hanscom Field, Bedford, Massachusetts
ATTN: CRXL, Technical Library

Commanding Officer, U.S. Army Communications & Electronics
Combat Development Agency, Fort Huachuca, Arizona
ATTN: Technical Library

Commanding Officer, U.S. Army Electronics Materiel Support Agency,
Fort Monmouth, New Jersey
ATTN: SELMS/ADJ
ATTN: SELMS/PFE-4 (Mr. L. Kramer)

Stanford Electronics Laboratories, Stanford University, Stanford, California
ATTN: Mr. J. Gibbons

University of Illinois, Urbana, Illinois
ATTN: Dr. J. Bardeen

Commander, Rome Air Development Center,
Air Research & Development Command, Griffiss Air Force Base, New York
ATTN: RAALD
ATTN: J. Naresky

Commanding Officer, U. S. Army Electronics R&D Activity,
White Sands Missile Range, New Mexico
ATTN: Mr. D. E. Samuelson

Commanding Officer, U.S. Army Electronics Research Unit,
P.O. Box 205, Mountain View, California

USAELRDL Liaison Office,
Detroit Arsenal, Center Line, Michigan

Commanding Officer, U.S. Army Chemical Research & Development Laboratories,
Edgewood Arsenal, Maryland
ATTN: Technical Library

Commanding General, U. S. Army Electronics Materiel Agency,
225 South 18th Street, Philadelphia 3, Pennsylvania
ATTN: SELMA-R2C (L. Schumann)

Director, National Bureau of Standards, Washington 25, D.C.
ATTN: Mr. J. C. French

Texas Instruments, Inc., P.O. Box 5012, Dallas 22, Texas
ATTN: Dr. Richard Petritz

Philco Corporation, C & Tioga Streets, Philadelphia 34, Pennsylvania

U.S. Naval Inspector of Ordnance, Applied Physics Laboratory,
The Johns Hopkins University, Silver Spring, Maryland

Bureau of Naval Weapons Representative, 1675 West 5th Street,
P.O. Box 1011, Pomona, California
ATTN: Metrology Department

Massachusetts Institute of Technology, 77 Massachusetts Avenue,
Cambridge 39, Massachusetts
ATTN: Tech. Documents Office

1 copy to each of the following:

Lincoln Laboratory, Massachusets Institute of Technology,
P.O. Box 73, Lexington 73, Massachusetts
ATTN: Group 85

Commander, N.Y. Naval Shipyard, Material Laboratory Library, Building 291,
Brooklyn 1, New York
ATTN: Code 911B

Sperry Gyroscope Company, Division of Sperry Rand Corporation,
Great Neck, Long Island, N. Y.
ATTN: Mr. F. Turnbull

Sage Laboratories, Inc., 3 Huron Drive, East Natick Industrial Park, Natick, Mass.
ATTN: Mr. T. Saad

Avco Corporation, Electronics & Ordnance Division,
2630 Glendale-Milford Road, Cincinnati 41, Ohio
ATTN: Technical Library

Harvard University, Tech. Reports Collection, 303A Pierce Hall,
Cambridge 38, Massachusetts
ATTN: Mr. M. L. Cox, Librarian

Sylvania Electric Products, Inc., 100 Sylvan Road, Woburn, Massachusetts
ATTN: Mr. S. G. Lawson

Radio Corporation of America, Sarnoff Research Center,
Princeton, New Jersey
ATTN: Mr. E. G. Linder

University of Pennsylvania,
Moore School of Electrical Engineering, Philadelphia, Pennsylvania
ATTN: Dr. Rubinoff

Purdue University, Physics Laboratory, Lafayette, Indiana
ATTN: Librarian
ATTN: Dr. H. Y. Fan

Northwestern University, 619 Clark Street, Evanston, Illinois
ATTN: Mr. R. E. Beam

University of Michigan, Willow Run Labs, Ypsilanti, Michigan
ATTN: Librarian (IRIA)

Purdue University, Electronics Engineering Division, West Lafayette, Indiana
ATTN: Mr. G. R. Cooper

Polytechnic Institute of Brooklyn, Graduate Center, Route 110, Farmingdale, N.Y.

Director, Cooley Electronics Laboratory,
University of Michigan, Ann Arbor, Michigan
ATTN: Dr. B. F. Barton

The Bendix Corporation, Eclipse-Pioneer Division, Teterboro, New Jersey
ATTN: Harold Moreines, Department 7211

Connecticut Telephone & Electric Corporation of Meriden,
38 Elm Street, Meriden, Connecticut

International Business Machines Corporation, Components Division,
P.O. Box 110, Poughkeepsie, New York
ATTN: R. Counihan

1 copy to each of the following:

Dubrow Electronic Industries, Inc., 235 Penn Street, Burlington, New Jersey

Fairchild Stratos Corporation, Electronic Systems Division,
Wyandanch, L.I., New York
ATTN: Technical Library

ITT, Kellogg Communications Systems Department,
500 North Pulaski Road, Chicago 24, Illinois
ATTN: Mr. R. H. Maier

Lenkurt Electric Company, Inc., 1105 County Road, San Carlos, California
ATTN: Mr. E. K. Peterson

P. R. Mallory & Company, Inc., Indianapolis 6, Indiana
ATTN: Mr. C. R. Dowden

Raytheon Company, Semiconductor Library,
P.O. Box 280, Mountain View, California

Sprague Electric Company, North Adams, Massachusetts

Stelma, Inc., 200 Henry Street, Stamford, Connecticut

Transitron Electronic Corporation, 168 Albion Street, Wakefield, Massachusetts
ATTN: Dr. Bakalar

Clevite Transistor, 241 Crescent Street, Waltham 54, Massachusetts

Vice President, Research and Engineering Department,
Western Union Telegraph Company, 60 Hudson Street, New York 13, New York
ATTN: Mr. C. M. Brown

Pacific Semiconductors, Inc., 14520 South Aviation Boulevard, Lawndale, Calif.
ATTN: Mr. R. M. Wood

Vitro Laboratories, Vitro Corporation of America, Silver Spring Laboratory,
14000 Georgia Avenue, Silver Spring, Maryland
ATTN: Miss C. Marian Jaques, Librarian

Cutler-Hammer, Airborne Instruments Laboratory Division,
Melville, Long Island, New York
ATTN: Library

Motorola, Inc., Semiconductor Products Division, 5005 East McDowell Road,
Phoenix, Arizona
ATTN: J. S. Larue

Shockley Transistor, Unit of Clevite Transistor,
Stanford Industrial Park, Palo Alto, California
ATTN: Dr. W. Shockley

Sperry Semiconductor, Division of Sperry Rand Corporation,
380 Main Avenue, Norwalk, Connecticut
ATTN: Library

Director, National Aeronautics and Space Administration,
Goddard Space Flight Center, Greenbelt, Maryland
ATTN: Mr. George Hogan, Code 652
ATTN: Mr. I. J. Ross, Code 650.1

1 copy to each of the following:

New York University, College of Engineering,
401 West 205th Street, New York 34, New York
ATTN: Project SETE

Hughes Aircraft Company, Semiconductor Division,
P.O. Box 278, Newport Beach, California
ATTN: Library

Director, Jet Propulsion Laboratory, California Institute of Technology,
4800 Oak Grove Drive, Pasadena, California

Battelle Memorial Institute, 505 King Avenue, Columbus 1, Ohio
ATTN: Main Library

Radio Corporation of America, Semiconductor Division, Somerville, New Jersey
ATTN: Patricia M. Kuran, Librarian

Commanding General, U. S. Army Missile Command,
Redstone Arsenal, Alabama
ATTN: AMSMI-MDE
ATTN: AMSMI-IHEE

Fairchild Semiconductor Corporation, 545 Whisman Road, Mountain View, California
ATTN: Mr. T. H. Bay

Commanding Officer & Director, U.S. Navy Electronics Laboratory,
San Diego 52, California

Deputy President, U.S. Army Security Agency Board,
Arlington Hall Station, Arlington 12, Virginia

Rheem Semiconductor Corporation, 350 Ellis Street, Mountain View, California
ATTN: Mr. C. A. Bittmann

Stanford Research Institute, Menlo Park, California
ATTN: External Reports, G-037

Electro-Optical Systems, Inc.,
300 North Halstead Street, Pasadena, California
ATTN: I. Welman

The Boeing Company, Aerospace Division, P.O. Box 3707,
Seattle 24, Washington
ATTN: Mr. G. S. Szekely

The Rand Corporation, 1700 Main Street, Santa Monica, California

Department of the Navy, Bureau of Ships, Washington 25, D.C.
ATTN: A. H. Young, Semiconductors Group, Code 681 AIA

Corps of Engineers Liaison Office,
U.S. Army Electronics R & D Laboratory, Fort Monmouth, New Jersey

AFSC Scientific/Technical Liaison Office,
U.S. Naval Air Development Center, Johnsville, Pennsylvania

Marine Corps Liaison Office,
U.S. Army Electronics R & D Laboratory, Fort Monmouth, New Jersey

OASD (R & E), Rm 1065, The Pentagon, Washington 25, D.C.
ATTN: Technical Library

Commanding Officer, Harry Diamond Laboratories, Washington 25, D.C.
ATTN: Library, Rm. 211, Bldg. 92

1 copy to each of the following:

Director, Fort Monmouth Office,
U.S. Army Communications & Electronics Combat Development Agency,
Fort Monmouth, New Jersey

Headquarters, Electronic Systems Division
L.G. Hanscom Field, Bedford, Massachusetts
ATTN: ESAT

Commander, Air Force Command & Control Development Division,
L. G. Hanscom Field, Bedford, Massachusetts
ATTN: CRZC

Commanding General, Aeronautical Systems Division,
Wright-Patterson Air Force Base, Ohio
ATTN: R. D. Alberts (ASRNEM)

Commander, Aeronautical Systems Division,
Wright-Patterson Air Force Base, Ohio
ATTN: ASAPRL

Chief of Research & Development, OCS, Dept. of the Army
Washington 25, D. C.

Commanding General, U.S. Army Material Command,
Washington 25, D. C.
ATTN: R & D Directorate

Commanding General, U.S. Army Combat Developments Command,
Fort Belvoir, Virginia
ATTN: CDCMR-E

WESTERN ELECTRIC COMPANY

A. E. Anderson (Allentown)
H. T. Ruberg
G. G. Kreider
L. C. Jarvis (3)

BELL TELEPHONE LABORATORIES

100 copies

This contract is supervised by the Solid State & Frequency Control Division, Electronic Components Department, USAELRDL, Fort Monmouth, New Jersey. For further information contact: Dr. Lothar Wandinger, Project Advisor, Telephone 535-1723.

AD________________ Accession No._____

Bell Telephone Laboratories, Inc., Murray Hill, N.J.

Engineering Services on Transistors
Report No. 10, First Quarterly Progress Report, 31 December 1962
Period, 1 August to 31 October 1962
Contract DA 36-039 sc-90759 (Unclassified)

Prepared by: J.H. Forster A.B. Kuper K.E. Martersteck T.B. Ramachandran J. Kocsis R. Lindner J.T. Nelson

68 pp, incl. 28 illus, 2 tables

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, with a view toward demonstrating and increasing the practicability of their use in operating equipment. This is a continuation of the work performed on Contract DA 36-039 sc-89201 and predecessor contracts.

This report discusses the work on microwave germanium transistors and integrated circuit devices.

Work on the germanium 1-Gc power transistor and the 3-Gc transistor has continued. Fabrication of 0.25 watt, 1-Gc mesa transistor models has been started. Problems of oxide breakdown in the planar structure and the possible use of photolithographic techniques and thermally deposited oxides are discussed. Techniques for reduction of base resistance are suggested. An analysis and some experimental results relating to the theory of high frequency base impedance of microwave transistors are given. Results indicate that a complex base impedance should be used in the equivalent circuit characterization. Analysis of the problem of charge distribution in the base and collector barrier regions of microwave transistors has been extended.

Status of the integrated circuit program is reviewed. The program now includes work on integration of diffused-silicon resistors or thin-film resistors with planar diffused-silicon devices. Operation of the multijunction diode level shifter in LLL gates is reviewed. It is concluded that satisfactory input margins for many applications are afforded with a double-junction level shifter used with an epitaxial 2N914 transistor.

UNCLASSIFIED

1. Engineering Services on Transistors, Report No. 10, First Quarterly Progress Report
2. Contract DA 36-039 sc-90759

AD________________ Accession No._____

Bell Telephone Laboratories, Inc., Murray Hill, N.J.

Engineering Services on Transistors
Report No. 10, First Quarterly Progress Report, 31 December 1962
Period, 1 August to 31 October 1962
Contract DA 36-039 sc-90759 (Unclassified)

Prepared by: J.H. Forster A.B. Kuper K.E. Martersteck T.B. Ramachandran J. Kocsis R. Lindner J.T. Nelson

68 pp, incl. 28 illus, 2 tables

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, with a view toward demonstrating and increasing the practicability of their use in operating equipment. This is a continuation of the work performed on Contract DA 36-039 sc-89201 and predecessor contracts.

This report discusses the work on microwave germanium transistors and integrated circuit devices.

Work on the germanium 1-Gc power transistor and the 3-Gc transistor has continued. Fabrication of 0.25 watt, 1-Gc mesa transistor models has been started. Problems of oxide breakdown in the planar structure and the possible use of photolithographic techniques and thermally deposited oxides are discussed. Techniques for reduction of base resistance are suggested. An analysis and some experimental results relating to the theory of high frequency base impedance of microwave transistors are given. Results indicate that a complex base impedance should be used in the equivalent circuit characterization. Analysis of the problem of charge distribution in the base and collector barrier regions of microwave transistors has been extended.

Status of the integrated circuit program is reviewed. The program now includes work on integration of diffused-silicon resistors or thin-film resistors with planar diffused-silicon devices. Operation of the multijunction diode level shifter in LLL gates is reviewed. It is concluded that satisfactory input margins for many applications are afforded with a double-junction level shifter used with an epitaxial 2N914 transistor.

UNCLASSIFIED

1. Engineering Services on Transistors, Report No. 10, First Quarterly Progress Report
2. Contract DA 36-039 sc-90759

AD________________ Accession No._____

Bell Telephone Laboratories, Inc., Murray Hill, N.J.

Engineering Services on Transistors
Report No. 10, First Quarterly Progress Report, 31 December 1962
Period, 1 August to 31 October 1962
Contract DA 36-039 sc-90759 (Unclassified)

Prepared by: J.H. Forster A.B. Kuper K.E. Martersteck T.B. Ramachandran J. Kocsis R. Lindner J.T. Nelson

68 pp, incl. 28 illus, 2 tables

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, with a view toward demonstrating and increasing the practicability of their use in operating equipment. This is a continuation of the work performed on Contract DA 36-039 sc-89201 and predecessor contracts.

This report discusses the work on microwave germanium transistors and integrated circuit devices.

Work on the germanium 1-Gc power transistor and the 3-Gc transistor has continued. Fabrication of 0.25 watt, 1-Gc mesa transistor models has been started. Problems of oxide breakdown in the planar structure and the possible use of photolithographic techniques and thermally deposited oxides are discussed. Techniques for reduction of base resistance are suggested. An analysis and some experimental results relating to the theory of high frequency base impedance of microwave transistors are given. Results indicate that a complex base impedance should be used in the equivalent circuit characterization. Analysis of the problem of charge distribution in the base and collector barrier regions of microwave transistors has been extended.

Status of the integrated circuit program is reviewed. The program now includes work on integration of diffused-silicon resistors or thin-film resistors with planar diffused-silicon devices. Operation of the multijunction diode level shifter in LLL gates is reviewed. It is concluded that satisfactory input margins for many applications are afforded with a double-junction level shifter used with an epitaxial 2N914 transistor.

UNCLASSIFIED

1. Engineering Services on Transistors, Report No. 10, First Quarterly Progress Report
2. Contract DA 36-039 sc-90759

AD________________ Accession No._____

Bell Telephone Laboratories, Inc., Murray Hill, N.J.

Engineering Services on Transistors
Report No. 10, First Quarterly Progress Report, 31 December 1962
Period, 1 August to 31 October 1962
Contract DA 36-039 sc-90759 (Unclassified)

Prepared by: J.H. Forster A.B. Kuper K.E. Martersteck T.B. Ramachandran J. Kocsis R. Lindner J.T. Nelson

68 pp, incl. 28 illus, 2 tables

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, with a view toward demonstrating and increasing the practicability of their use in operating equipment. This is a continuation of the work performed on Contract DA 36-039 sc-89201 and predecessor contracts.

This report discusses the work on microwave germanium transistors and integrated circuit devices.

Work on the germanium 1-Gc power transistor and the 3-Gc transistor has continued. Fabrication of 0.25 watt, 1-Gc mesa transistor models has been started. Problems of oxide breakdown in the planar structure and the possible use of photolithographic techniques and thermally deposited oxides are discussed. Techniques for reduction of base resistance are suggested. An analysis and some experimental results relating to the theory of high frequency base impedance of microwave transistors are given. Results indicate that a complex base impedance should be used in the equivalent circuit characterization. Analysis of the problem of charge distribution in the base and collector barrier regions of microwave transistors has been extended.

Status of the integrated circuit program is reviewed. The program now includes work on integration of diffused-silicon resistors or thin-film resistors with planar diffused-silicon devices. Operation of the multijunction diode level shifter in LLL gates is reviewed. It is concluded that satisfactory input margins for many applications are afforded with a double-junction level shifter used with an epitaxial 2N914 transistor.

UNCLASSIFIED

1. Engineering Services on Transistors, Report No. 10, First Quarterly Progress Report
2. Contract DA 36-039 sc-90759

AD_____ Accession No. _____

Bell Telephone Laboratories, Inc., Murray Hill, N.J.

MICROWAVE DIODE RESEARCH
Report No. 11, Second Quarterly Progress Report, 10 March 1963
Period, 10 September to 9 December 1962
Contract DA 36-039 sc-89205
32 pp. incl. 8 illus, 2 tables

Prepared by: L. A. D'Asaro, W. S. Khokley

The general objective of this contract is to make theoretical and experimental studies leading toward exploratory development of new microwave crystal diodes.

A survey of the present day status of Esaki diode microwave receivers is presented. The factors considered are noise figure, stability, dynamic range, gain-band product, phase and amplitude distortion and device reliability. Criteria for stability have been given which should aid in the design of suitable encapsulations. The presently available noise figure of a typical GaSb Esaki diode receiver at 1 Gc is about 4 db, with 16-db gain in the first stage. The maximum input power, limited by 1-db compression in gain, is about -49 dbm. The gain-band product of the Esaki diodes presently available for such receivers is about 6 Gc. An Esaki diode down-converter used as the first stage of a microwave receiver is expected to have about the same noise figure as the amplifier, more critical adjustments and a dynamic range 3 db larger. A comparison of the characteristics of Esaki diode microwave receivers with other microwave receivers shows that the principal advantage of the Esaki diode receivers is their expected low cost, due to the absence of a pump oscillator or refrigeration. Therefore, the Esaki diode receiver may be useful where cost is important and the other properties of the receiver are suitable. The dynamic range of present day Esaki diode receivers is shown to be adequate for certain cases, and can be somewhat widened by using lower-impedance devices yet to be developed.

UNCLASSIFIED

1. Microwave Diode Research Report No. 11, Second Quarterly Progress Report
2. Contract DA 36-039 sc-89205

AD_____ Accession No. _____

Bell Telephone Laboratories, Inc., Murray Hill, N.J.

MICROWAVE DIODE RESEARCH
Report No. 11, Second Quarterly Progress Report, 10 March 1963
Period, 10 September to 9 December 1962
Contract DA 36-039 sc-89205
32 pp. incl. 8 illus, 2 tables

Prepared by: L. A. D'Asaro, W. S. Khokley

The general objective of this contract is to make theoretical and experimental studies leading toward exploratory development of new microwave crystal diodes.

A survey of the present day status of Esaki diode microwave receivers is presented. The factors considered are noise figure, stability, dynamic range, gain-band product, phase and amplitude distortion and device reliability. Criteria for stability have been given which should aid in the design of suitable encapsulations. The presently available noise figure of a typical GaSb Esaki diode receiver at 1 Gc is about 4 db, with 16-db gain in the first stage. The maximum input power, limited by 1-db compression in gain, is about -49 dbm. The gain-band product of the Esaki diodes presently available for such receivers is about 6 Gc. An Esaki diode down-converter used as the first stage of a microwave receiver is expected to have about the same noise figure as the amplifier, more critical adjustments and a dynamic range 3 db larger. A comparison of the characteristics of Esaki diode microwave receivers with other microwave receivers shows that the principal advantage of the Esaki diode receivers is their expected low cost, due to the absence of a pump oscillator or refrigeration. Therefore, the Esaki diode receiver may be useful where cost is important and the other properties of the receiver are suitable. The dynamic range of present day Esaki diode receivers is shown to be adequate for certain cases, and can be somewhat widened by using lower-impedance devices yet to be developed.

UNCLASSIFIED

1. Microwave Diode Research Report No. 11, Second Quarterly Progress Report
2. Contract DA 36-039 sc-89205

UNCLASSIFIED